TI-PMLK

TI Power Management Lab Kit
LDO Experiment Book

Texas Instruments

SSQU006B
PMLKLDOEVM REV B

Texas Instruments

Name

University/Company name

Address

Phone

E-mail

Many people have collaborated with me in the realization of the TI-PMLK project, in different times, at different levels, in different ways. My sincerest thanks go to the Texas Instruments University Program Team and to the University of Salerno Power Electronics Laboratory Team.

Nicola Femia

Preface

Felix, qui potuit rerum cognoscere causas...
(Happy, he who could capture the origins of things...)
Publio Virgilio Marone, Mantova 70 B.C. – Brindisi 19 B.C.

Design is an exciting and fascinating art. Power electronics, for its interdisciplinarily nature, is a challenging field where the knowledge of *why* makes all the difference in understanding *how* to achieve design goals. The *will of learning* and the *means for learning* are the two basic ingredients needed to develop the virtuous ability to understand the reality of problems, to select the appropriate techniques and methods to solve them, to make meaningful design decisions and to intelligently evaluate the solutions.

The main purpose of the TI-PMLK collection of Experiment Books is to stimulate the spirit of investigation in students and practicing engineers who are engaged in learning and understanding the design of power supplies. The experiments cover a basic anthology of topics and issues encountered in the design of low power dc-dc non-isolated power supplies, such as power supplies topologies and characteristics, modes of operation, efficiency, control, stability, accuracy, transient response, noise, power magnetics, and more. The experiments can be performed by using the power supply boards of the TI-PMLK suite, which includes low dropout linear regulators and buck, boost and buck-boost switching regulators. The Experiment books are not intended to provide an exhaustive overview of design issues or definitive design hints: rather, it is meant to guide the reader into a multifaceted active learning experience.

All the experiments are based on a logical sequence of steps. They start with the *Case Study* section, which provides the description of the specific property or feature relevant to the power supply board to be used in the experiment, and illustrates the goal and the type of measurement to be done. The *Theory Background* section provides a short summary of concepts, models and equations, supporting the interpretation and understanding of the incoming experimental observations. The *Measurement Setup* section provides the instructions for connecting the instruments needed for the experiments to the board under test. Warnings are provided to prevent main mistakes. The *Test* section provides instructions on how to execute the measurements, and guidelines on how to analyze and understand the results of the measurements. Each test includes an *Answer* section, where the user is required to answer questions and to provide a discussion about the behavior of the board under test, relevant to the specific performance under investigation, based on the observation of the measurements results and on the application of concepts and properties illustrated through the various sections of the experiment. The *Discussion* section provides comments to achieve a better understanding of conceptual and practical correlations among system characteristics and operating performance. The final *Experimental Plots* section illustrates and discusses the results of some sample measurements.

Preface (cont.)

The experiments cover a variety of steady-state, transient and dynamic tests. The tests are mostly based on time domain measurements, while some tests focus on the investigation of dynamic properties that are described through frequency response functions, such as the power supply rejection ratio. This allows a user to conduct a complete experience on the characterization and understanding of power supply issues. Most of the experiments require basic laboratory equipment, including a power supply, some multi-meters, an oscilloscope and a load. Some tests require more sophisticated instrumentation, such as a dynamic source, a dynamic load, and a vector network analyzer, for best measurement.

The boards have been designed to allow the investigation of the influence of physical parameters and operating conditions of a power supply on its own performances. Various combinations of power and control components can be selected. Most of them yield operating conditions that fit good engineering standards. Other ones may lead to operating conditions typically undesired in industry applications, such as instability. Thus, the reader can achieve a sound understanding of such real phenomena.

Suggested combinations of power and control parts are provided for each experiment. The user is invited in some experiments to detect combinations that yield a certain operating condition or behavior. The user can select the setup of jumpers and connectors to generate a great variety of conditions. The book provides recommendations and warnings for safe board operation and for effective measurements. Before performing any experiment, the reader is strongly recommended to read carefully all the warnings and the introductory section of the book, where the specific description of the board is provided and information on settings and performance are given, including forbidden combinations and special operating conditions. The reader is also strongly invited to read the manufacturers' datasheets of all the parts mounted in the boards, especially the control chips, to improve the knowledge and the understanding of each device.

A good knowledge of the power supplies implemented on the boards, supported by the heuristic observations and the models and methods discussed in the book, help the user to distinguish what can be done from what cannot be done.

The level of detail and completeness of models discussed in the *Theory Background* section vary from experiment to experiment. Sometimes the models include certain specific properties, other times they are simplified or approximated. Achieving familiarity with models is a fundamental learning step: a good power supply designer has to be able to grade the importance of modeling certain properties, at device level as well as at system level, in order to assess if they really provide meaningful and influential information to meet the application requirements. Essential formulas and expressions for the basic analysis of the phenomenon under investigation are mostly introduced without step-by-step theoretical derivations, which are beyond the objectives of the book.

The reader is encouraged to test him(her)self in filling this gap, through an in-depth study of models and methods for the analysis and design of power supplies discussed in the cited references.

Preface (cont.)

The parameters of semiconductor and passive power components mounted on the boards are provided in the book to allow the application of analysis formulas and design equations. All parameters of power components are affected by uncertainty, due to tolerances, ageing and influence factors like temperature, current, voltage and frequency. The values collected in the books have been extracted from the manufacturers' datasheets in certain reference conditions. The power and control components and sub-circuits of integrated circuits controlling the power supplies, which determine modes of operation and performances, are subjected to the influence of temperature, voltage, current and frequency too. As a consequence, the predictions of formulas and equations provided in the book, based on the parameters of power and control devices, can show different levels of agreement with respect to the results of experimental measurements.

The user is strongly encouraged to read the references provided in the book, to analyze the characteristics and the behavior of integrated circuits and power components of the boards, and to verify if different values of the parameters of components can be used to achieve a better compliance between the results of formulas and the results of experimental measurements. The investigation of real device characteristics and of their influence on overall performance of a power supply is a fundamental component of designers' work.

The ultimate intention of this book is to accompany the reader through an active experience, made of observations, application of physics and mathematics, reality investigation and system level reasoning. That is engineering insight. The Author hopes the reader may fully enjoy this book and the pleasure of being a design engineer, a creative and autonomous thinker, able to acquire and re-elaborate the knowledge to win ever new design challenges.

Know why, know how!

Nicola Femia

Nicola Femia is Professor at the University of Salerno, Italy, where he teaches Power Electronics and Energetic Intelligence, in the Electronic Engineering and Computer Engineering Master Degree Programs. He leads the Power Electronics and Renewable Sources Laboratory. Over the past 25 years, he has promoted and directed worldwide university and industry research activities and education programs on power electronics, photovoltaic systems, and power design. He has been Visiting Professor at the Electrical Engineering Department of the Stanford University, Stanford, CA, where he taught Power Electronics Control and Energy Aware Design.

e-mail: *femia@unisa.it;*
web: *www.unisa.it/docenti/nicolafemia/index*

Table of Contents

Preface 7

Instrumentation needed for Experiments 13

TI-PMLK LDO TPS7A4901 description

- *Schematic* 16
- *Bill of Materials* 17
- *Board* 18
- *Connectors, Jumpers and Test Pins* 19

TI-PMLK LDO TPS7A8300 description

- *Schematic* 20
- *Bill of Materials* 21
- *Board* 22
- *Connectors, Jumpers and Test Pins* 23

Notes, Warnings and Recommendations. 24

Experiment 1

Impact of line and load conditions on drouput voltage 25

Experiment 2

Impact of line and load conditions on efficiency . . .37

Experiment 3

Impact of line and load conditions and output capacitor on stability and transient response 49

Experiment 4

Impact of capacitors on Power Supply Rejection Ratio 61

Experiment 5

Impact of line and load conditions on dropout voltage 73

Experiment 6

Impact of output capacitor on load-transient response 85

Appendix A

References 97

Appendix B

Manufacturers websites. 98

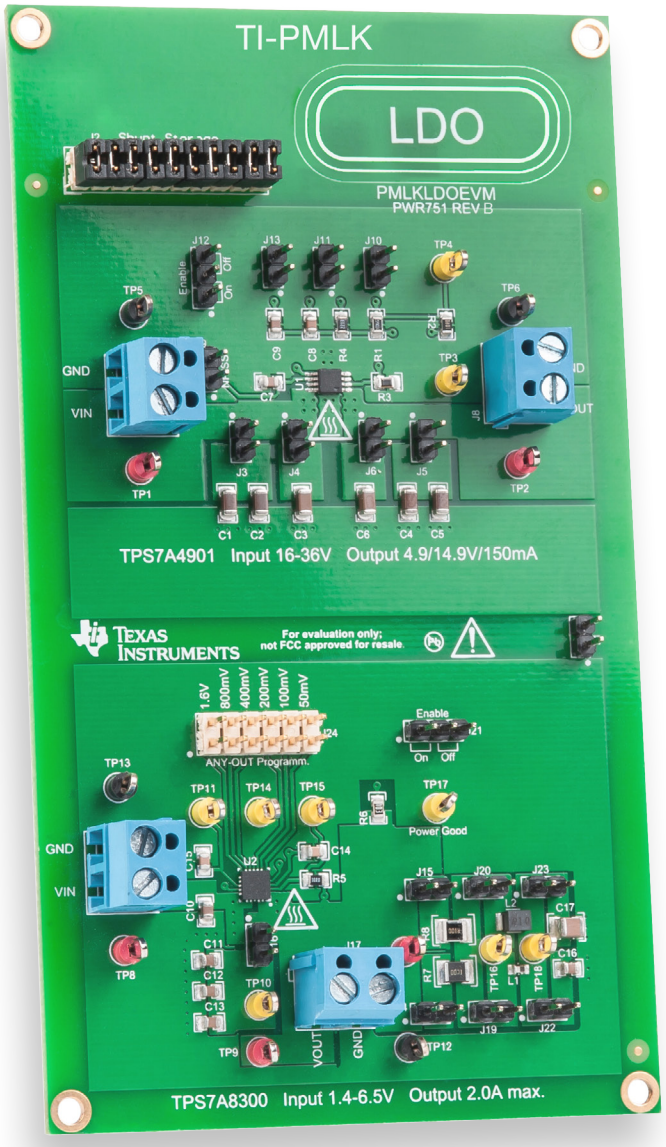
Instrumentation needed for experiments

The instrumentation recommended for the execution of the Experiments of this Book is comprised of:

- *DC power supply 0-50V/4A with dynamic voltage mode capability*
- *DC electronic load 20V/10A with dynamic current mode capability*
- *4 digital multimeters with 4½ digit resolution*
- *250MHz 4-channels Digital Oscilloscope + 2 current probes 20A/50MHz*
- *10Hz-10MHz Network Vector Analyzer with line injector*
- *10MHz Waveform Generator*

The instrumentation used in the lab tests corresponding to the Experimental Plot samples shown in the book is comprised of:

- *TTi EX354RT Power Supply 0-70V/4A* (*used in the experiments where the board under test had to be fed by a constant DC voltage source*)
- *Keithley 2420 SourceMeter, 63V, 3.15A* (*used in the experiments where the board under test had to be fed by a dynamic DC voltage source*)
- *Sorensen Electronic Load SLM-4 mainframe + SLM series electronic load modules 60V/60A*
- *LeCroy WaveRunner 44Xi 400MHz 4-channels Digital Oscilloscope, with 2 Tektronix TCP 305 50A current probe + Tektronix TCP A300 amplifier*
- *Omicron Bode 100 1Hz-40MHz Network Vector Analyzer with Picotest J2120A line injector* (*used in the experiment where the board under test had to be fed by a static DC voltage source with an AC noise injected*)
- *Agilent 33500b 30MHz Waveform Generator*



TI-PMLK-LDO

The TI-PMLK-LDO is an experimental power supply board based on two integrated linear voltage regulators, the ultra-low dropout TPS7A8300 and the ultra-low noise TPS7A4901

TI-PMLK TPS7A4901 Schematic

The TI-PMLK TPS7A4901 section of the board accepts input voltages in between 6V and 36V, while regulating output voltage at 5V or 15V with a maximum load current 150mA.

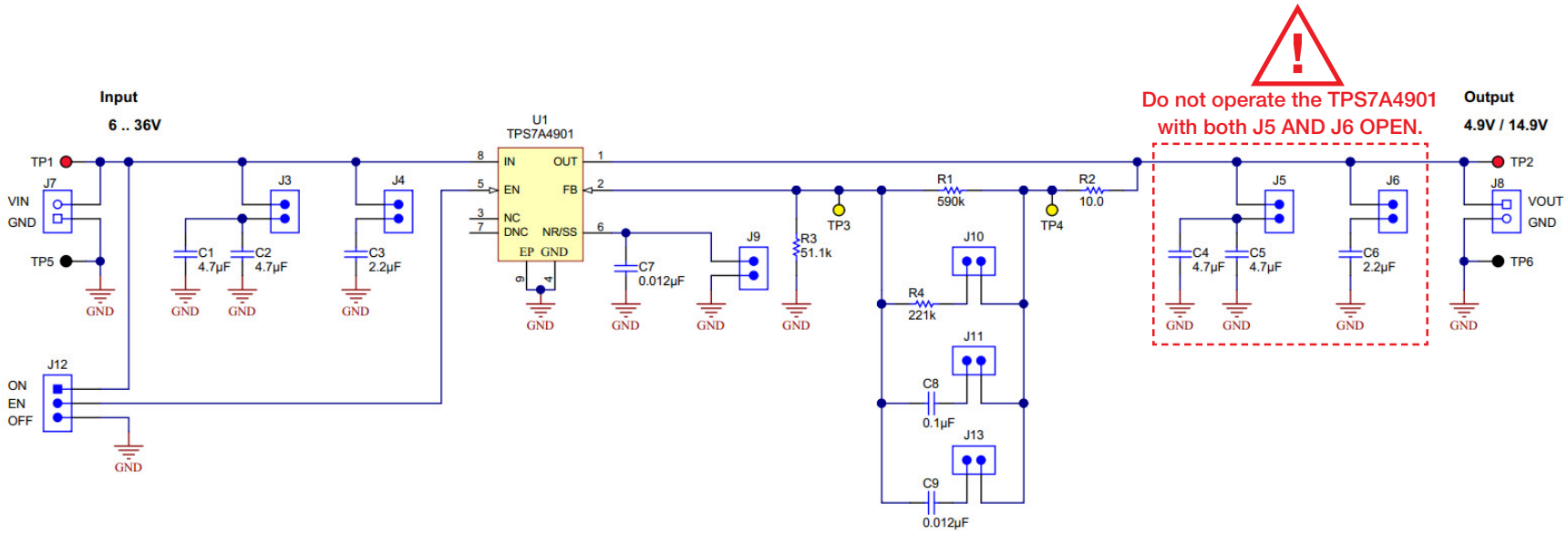


Figure 1. Circuit schematic of TI-PMLK TPS7A4901 LDO regulator

TI-PMLK TPS7A4901 Bill of Materials

Designator	Description	Manufacturer	Part Number
C1, C2, C4, C5	ceramic capacitor, 4.7µF, 50V, +/-10%, X7R, 1206	Taiyo Yuden	UMK316AB7475KL-T
C3, C6	ceramic capacitor, 2.2µF, 50V, +/-10%, X7R, 1206	MuRata	GRM31CR71H225KA88L
C7, C9	ceramic capacitor, 0.012µF, 50V, +/- 10%, X7R, 0805	AVX	08055C123KAT2A
C8	ceramic capacitor, 0.1µF, 50V, +/- 10%, X7R, 0805	Kemet	C0805C104K5RACTU
R1	resistor, 590kΩ, 1%, 0.125W, 0805	Panasonic	ERJ-6ENF5903V
R2	resistor, 10.0Ω, 0.1%, 0.125W, 0805	Yageo America	RT0805BRD0710RL
R3	resistor, 51.1kΩ, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-5112-B-T5
R4	resistor, 221kΩ, 1%, 0.125W, 0805	Vishay-Dale	CRCW0805221KFKEA
U1	Single Output High PSRR LDO, 150mA, Adjustable 1.2 to 33V Output, 3 to 36V Input, with Ultra-Low Noise, 8-pin MSOP (DGN)	Texas Instruments	TPS7A4901DGNR

(*use the part numbers of components to retrieve, through the manufacturers websites listed in the references, details about parameters and data that are used in the formulae provided for calculations in each experiment*)

TI-PMLK TPS7A4901 Board

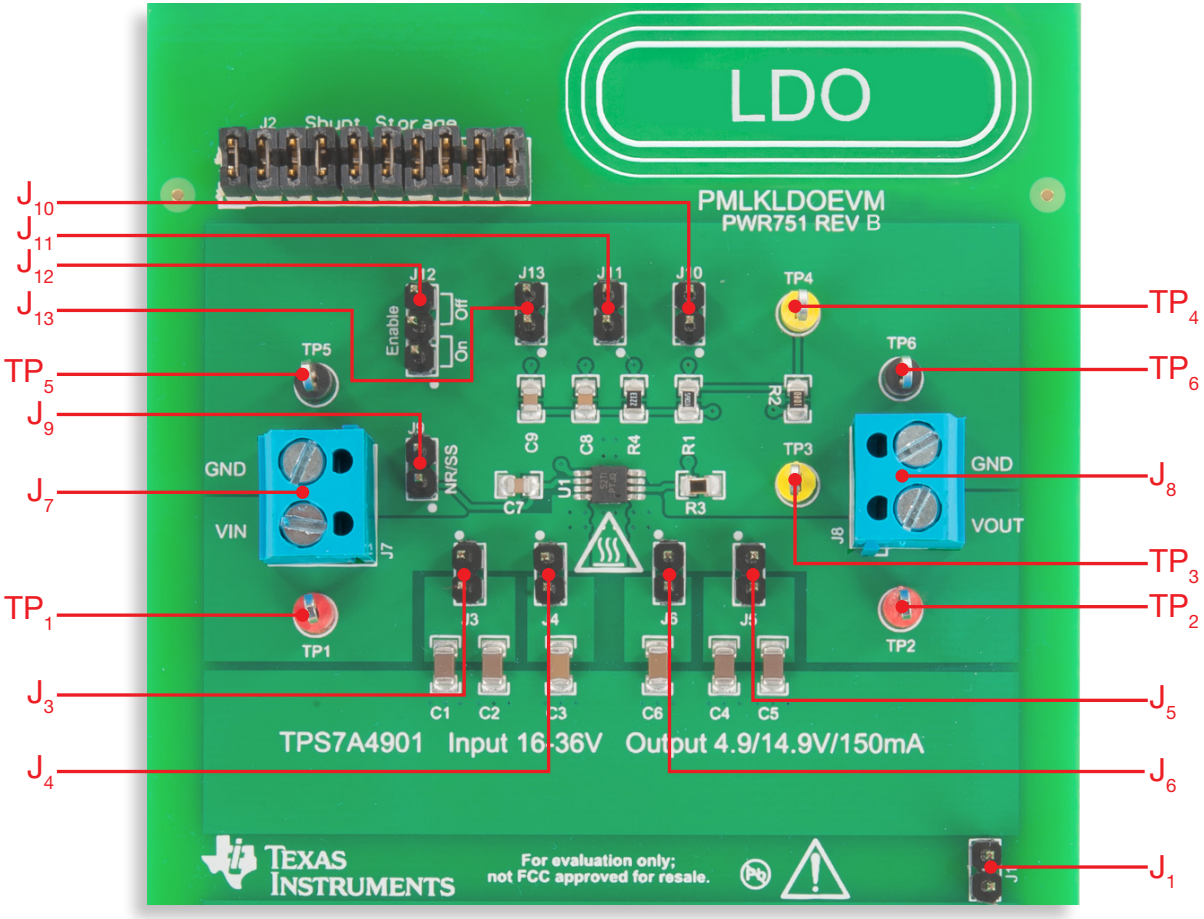


Figure 2. Plain view of TI-PMLK TPS7A4901 LDO regulator board

TI-PMLK TPS7A4901 Connectors, Jumpers and Test Pins

Descriptors and functions for Connectors, Jumpers and Test Pins

Connectors

J_7 - input voltage screw drive connector
J_8 - output voltage screw drive connector

Jumpers

J_1 - connects grounds of TPS7A4901 and TPS7A8300 board sections
J_3 - connects C_1 (4.7µF) and C_2 (4.7µF) input capacitors
J_4 - connects C_3 (2.2µF) input capacitor
J_5 - connects C_4 (4.7µF) and C_5 (4.7µF) output capacitors
J_6 - connects C_6 (2.2µF) output capacitor
J_9 - connects Noise Reduction/Soft Start pin directly to ground and shorts across C_7 (12nF) noise reduction capacitor
J_{10} - connects R_4 (221kΩ) resistor for 5V output voltage operation
J_{11} - connects C_8 (100nF) phase lead capacitor
J_{12} - enables LDO operation when top pin and center pin are shorted (ON), while it disables the LDO operation when center pin and bottom pin are shorted (OFF)
J_{13} - connects C_9 (12nF) phase lead capacitor

Test pins

TP_1 - positive pole of input voltage
TP_5 - ground pole of input voltage
TP_2 - positive pole of output voltage
TP_6 - ground pole of output voltage
TP_3 - feedback voltage
TP_4 - pin for loop gain measurements, can be used together with TP_3 to inject the ac stimulus into the 10Ω resistor R_2

Voltage and Current Measurements

- use TP_1 and TP_5 to measure the input voltage
- use TP_2 and TP_6 to measure the output voltage
- use TP_3 and TP_6 to measure the feedback voltage
- hang a current probe to one of the external power wires connected to J_7 to measure the input current
- hang a current probe to one of the external power wires connected to J_8 to measure the load current

TI-PMLK TPS7A8300 Schematic

The TI-PMLK TPS7A8300 section of the board accepts input voltages in between 1.4V and 6.5V. The output voltage can be set between 0.8V and 3.95V with onboard jumpers on J_{24}, with a maximum load current of 2A.

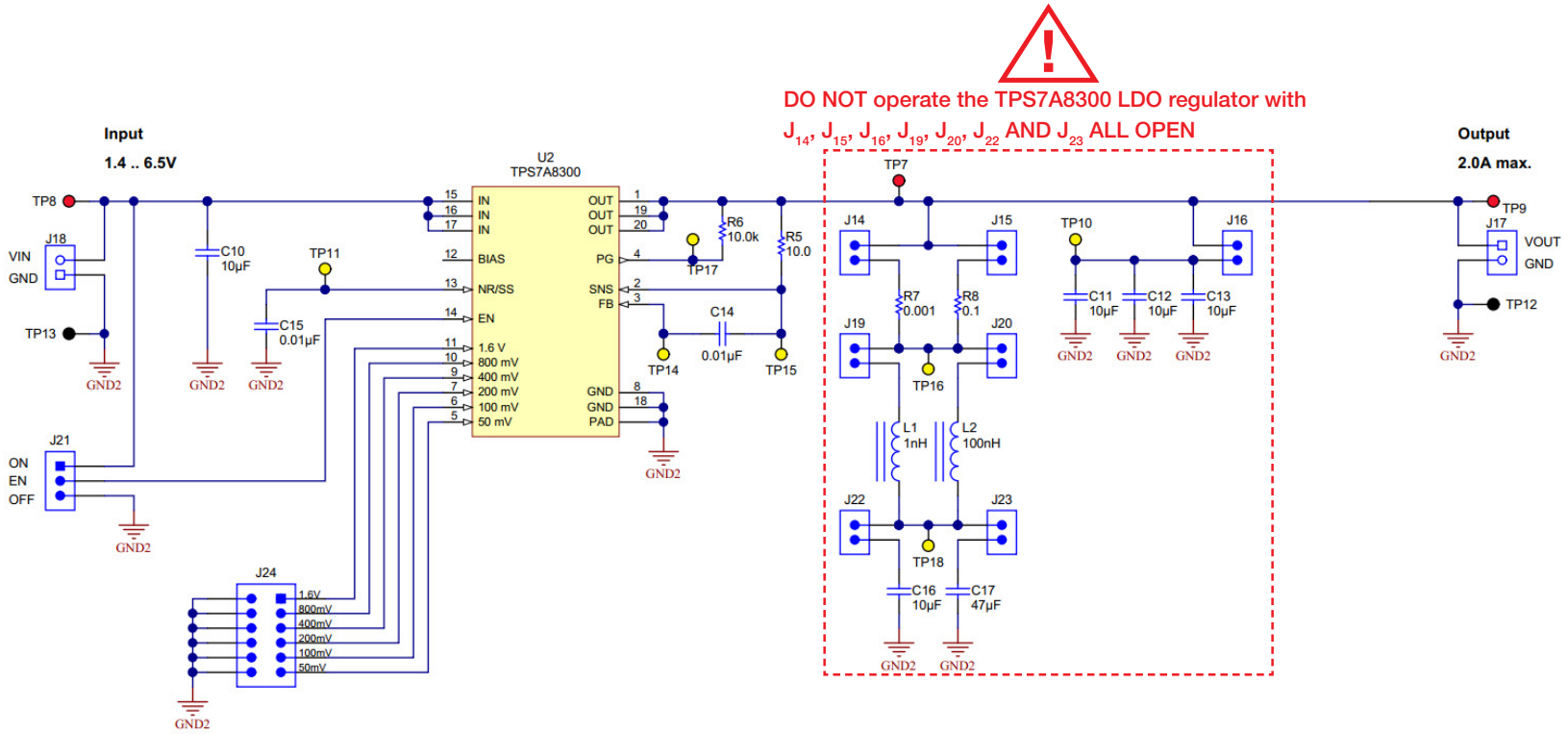


Figure 3. Circuit schematic of TI-PMLK TPS7A8300 LDO regulator

TI-PMLK TPS7A8300 Bill of Materials

Designator	Description	Manufacturer	Part Number
C10, C11, C12, C13, C16	ceramic capacitor, 10µF, 16V, +/-10%, X5R, 0805	MuRata	GRM21BR61C106KE15L
C14, C15	ceramic capacitor, 0.01µF, 50V, +/-10%, X7R, 0805	MuRata	GRM216R71H103KA01D
C17	ceramic capacitor, 47µF, 16 V, +/- 20%, X5R, 1210	MuRata	GRM32ER61C476ME15L
L1	Inductor, Multilayer, Ceramic, 1nH, 0.3A, 0.015Ω, SMD	Taiyo Yuden	HK16081N0S-T
L2	Inductor, Wirewound, Ferrite, 100nH, 2.85A, 0.02Ω, SMD	TDK	NLCV32T-R10M-PFR
R5	resistor, 10.0Ω, 1%, 0.125W, 0805	Yageo America	RC0805FR-0710RL
R6	resistor, 10.0kΩ, 0.1%, 0.125W, 0805	Yageo America	RT0805BRD0710KL
R7	resistor, 0.001Ω, 1%, 1W, 1210	Rohm	PMR25HZPFV1L00
R8	resistor, 0.1Ω, 1%, 0.5W, 1210	Rohm	MCR25JZHFLR100
U2	2-A, Low Noise, RF, LDO Voltage Regulator, 20-pin Plastic Quad Flatpack	Texas Instruments	TPS7A8300RGR

(*use the part numbers of components to retrieve, through the manufacturers websites listed in the references, details about parameters and data that are used in the formulae provided for calculations in each experiment*)

TI-PMLK TPS7A8300 Board

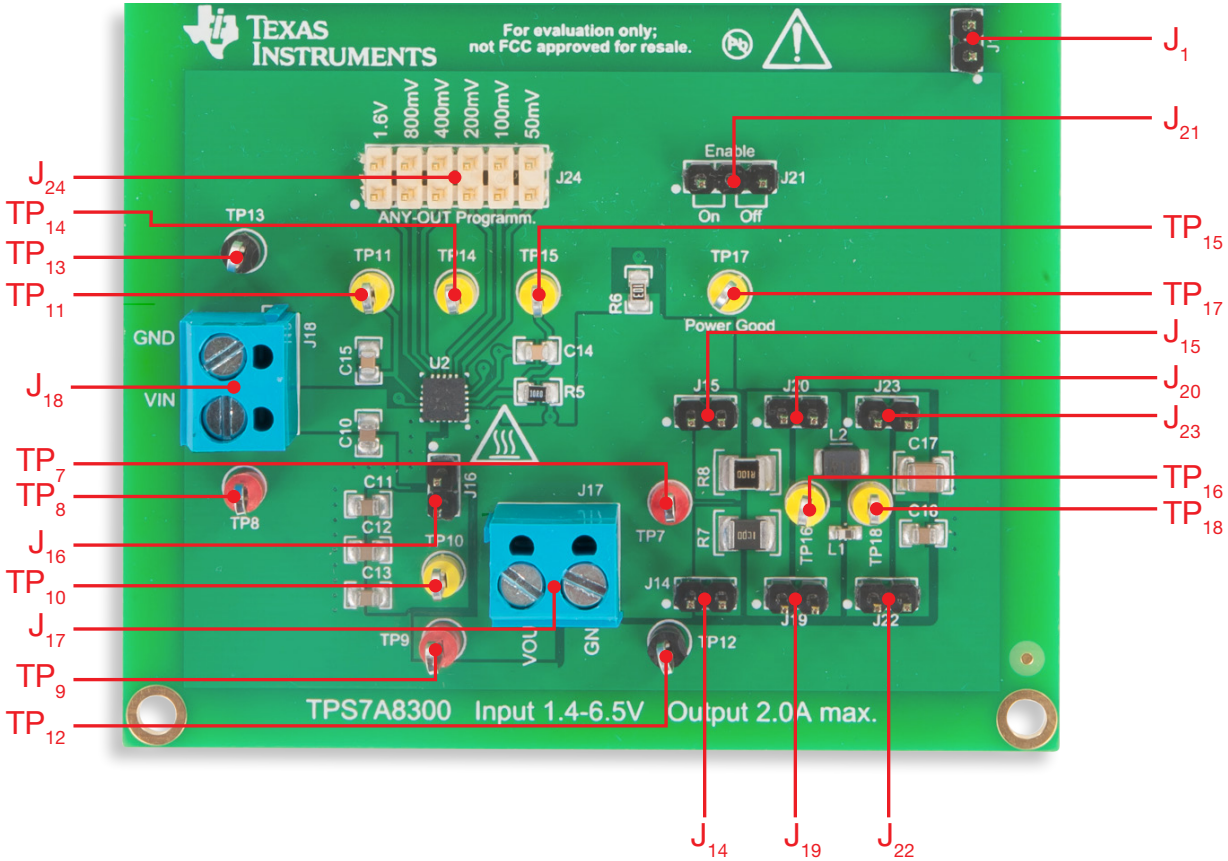


Figure 4. Plain view of TI-PMLK TPS7A8300 LDO regulator board

TI-PMLK TPS7A8300 Connectors, Jumpers and Test Pins

Descriptors and functions for Connectors, Jumpers and Test Pins

Connectors

J_{18} - input voltage screwdrive connector
J_{17} - output voltage screwdrive connector

Jumpers

J_{14} - connects the resistor R_7 (1mΩ) [emulated ESR]
J_{15} - connects the resistor R_8 (100mΩ) [emulated ESR]
J_{16} - connects the C_{11}- C_{13} (3x10µF) output capacitors
J_{19} - connects the inductor L_1 (1nH,15mΩ) [emulated ESL]
J_{20} - connects the inductor L_2 (100nH,20mΩ) [emulated ESL]
J_{21} - enables LDO operation when ON pin and EN pin are shorted, while it disables the LDO operation when EN pin and OFF pin are shorted
J_{22} - connects the output capacitor C_{16} (10µF)
J_{23} - connects the output capacitor C_{17} (47µF)
J_{24} - connects the internal resistors of TPS7A8300 to adjust the output voltage
J_1 - connects grounds of the TPS7A4901 and the TPS7A8300 board sections

Test pins

TP_8 - positive pole of input voltage
TP_9 - positive pole of output voltage
TP_{10} - voltage on C_{11}- C_{13} (3x10µF) output capacitors
TP_{11} - noise rejection capacitor voltage
TP_{12} - ground pole of output voltage
TP_{13} - ground pole of input voltage
TP_{14} - feedback voltage
TP_{15} - connection pin for loop gain measurements, can be used together with TP_7 to inject the AC stimulus into the 10Ω resistor R_5
TP_{16} - can be used together with TP_7 to sense the voltage across the resistors R_7 (1mΩ) and R_8 (100mΩ) [emulated ESR]
TP_{17} - Power Good pin voltage
TP_{18} - can be used together with TP_{16} to sense the voltage across inductors L_1 (1nH,15mΩ) and L_2 (100nH,20mΩ) [emulated ESL], or to sense the voltage across capacitors C_{16} (10µF) and C_{17} (47µF)

Voltage and Current Measurements

- use TP_8 and TP_{13} to measure the input voltage
- use TP_9 and TP_{12} to measure the output voltage
- use TP_{14} to measure the feedback voltage
- hang a current probe to one of the external power wires connected to J_{18} to measure the input current
- hang a current probe to one of the external power wires connected to J_{17} to measure the load current

Notes, Warnings and Recommendations

NOTES

- The jumper J_9 of the TPS7A4901 LDO regulator can be used to connect an external capacitor in parallel to the C_7 (12nF) NR/SS capacitor. Increasing the NR/SS capacitance determines a longer Soft Start time at the start-up, modifies the Power Supply Rejection Ratio (PSRR) and reduces the output voltage noise.

- The jumper J_{10} of the TPS7A4901 LDO regulator can be used to connect an external resistor in series to the R_4 (221kΩ) voltage divider resistor. Increasing the resistance in series to R_4 allows to increase the output voltage. The value of the resistance R_x to put in series to R_4 to get a value V_x of the output voltage V_{out} is given by the following formula:

$$R_x = \frac{R_1 R_3 (V_x - V_{ref})}{(R_1 + R_3) V_{ref} - R_3 V_x} - R_4$$

- The capacitor C_{16} (10µF) mounted in the TPS7A8300 board can be connected directly to the output of the TPS7A8300 LDO regulator by shorting the upside pin of the jumper J_{14} with the downside pin of the jumper J_{22}.

- The capacitor C_{17} (47µF) mounted in the TPS7A8300 board can be connected directly to the output of the TPS7A8300 LDO regulator by shorting the upside pin of the jumper J_{15} with the downside pin of the jumper J_{23}.

WARNINGS AND RECOMMENDATIONS

GENERAL

1) **DO NOT** exceed input and output voltage and current ratings
2) If the board is terminated at the output into an electronic load in constant current mode, the sequence to follow is:
   a) at the turn on: turn on the power supply, then turn on the electronic load
   b) at the turn off: turn off the electronic load, then turn off the power supply
3) Whatever change in the setup of jumpers has to be done, the board has to be shut down first, according to the recommendations given at point 2)
4) The board has to be operated at ambient temperature **25°C** (maximum **27.5°C)**

TPS7A4901 LDO REGULATOR

1) **DO NOT** operate the regulator with both J_5 **AND** J_6 **OPEN**
2) For an effective load transient response measurement, the use of an electronic load with high slew-rate (>1A/µs) dynamic current sink mode operation is recommended
3) For an effective line transient response measurement, a power supply with high slew-rate (>1V/µs) dynamic voltage mode operation is suggested
4) In the test of PSRR, if a power summing amplifier is used to inject into the input the ac stimulus, be sure that the total dc+ac input voltage never exceeds the maximum voltage rating of the board and that it does not become negative

TPS7A8300 LDO REGULATOR

1) If J_{16} is **OPEN**, one of the two capacitors C_{16} or C_{17} has to be connected to the output, through J_{22} or J_{23}, to one of the two resistors R_7 and R_8, through J_{14} and J_{15}, and to one of the inductors L_1 and L_2, through J_{19} and J_{20}
2) For an effective load transient response measurement, the use of an electronic load with high slew-rate (>1A/µs) dynamic current sink mode operation is recommended

Experiment 1

The goal of this experiment is to analyze how the output voltage regulation capabilities of an LDO regulator depend on the line and load conditions. The TPS7A4901 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze how the dropout voltage and the output voltage accuracy of an LDO regulator depend on the line and load conditions.

Figure 1 shows the simplified schematic of the TPS7A4901 LDO regulator. Two elements characterize the **regulation capability** of the LDO regulator: the **regulation region** and the **regulation accuracy**. The regulation region is identified by the input voltage range [V_{INmin},V_{INmax}] and the output current range [I_{OUTmin},I_{OUTmax}] wherein the LDO is able to regulate the output voltage. The output current range spans from ~0A to a maximum current I_{OUTmax}, which is determined by the maximum temperature rating of the LDO, the power dissipation capabilities of its package and the maximum input voltage of the LDO (I_{OUTmax}=150mA for TPS7A4901). The output voltage range spans from the dropout voltage V_{DO} =V_{INmin}, that depends on the pass device characteristics, to a maximum V_{INmax}, that depends on chip technology (V_{INmax}=36V for TPS7A4901). The regulation accuracy of the LDO regulator is the percent tolerance (V_{out}-V_{outnom})/V_{outnom}x100 of the output voltage V_{out} with respect to the nominal value V_{outnom}. The regulation accuracy depends on the **load regulation** and **line regulation,** which is expressed as the output voltage tolerance versus the load current I_{OUT} and versus the input voltage V_{IN}, over the relevant regulation ranges [I_{OUTmin},I_{OUTmax}] and [V_{INmin},V_{INmax}].

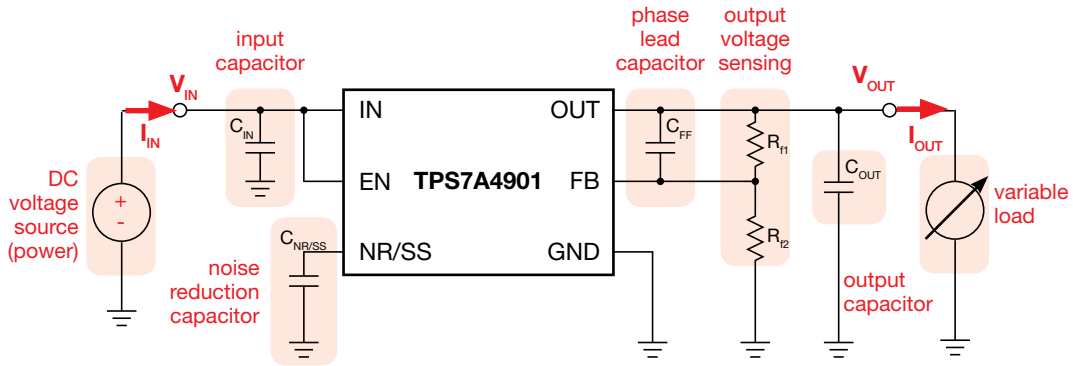


Figure 1. Simplified schematic of the TPS7A4901 LDO regulator

Test#1. We measure the input voltage and the output voltage of the TPS7A4901 LDO regulator while varying the load current. The goal is to determine the dropout voltage of the LDO regulator. To detect the value of the dropout voltage we decrease the input voltage, starting from a value that is sufficiently bigger than the output voltage, and observe the output voltage to see when it begins decreasing with respect to its nominal value. While the input voltage decreases, the operating point of the LDO regulator moves along the curve of Fig.4, sliding from the *regulation region* to the *dropout region*.

Test#2. We measure the output voltage of the TPS7A4901 LDO regulator while varying the load current and the line voltage. The goal is to verify the regulation capabilities of the LDO regulator when it is in the regulation region, and to observe if and how the output voltage depends on the load current and line voltage. To verify the regulation capabilities we make two type of measurements. First, we set the input voltage of the LDO regulator at a value higher than the dropout voltage investigated in the previous test, we observe the output voltage while varying the load current, and determine the *load regulation*. Then, we set the load current at a given value and observe the output voltage while varying the input voltage, and determine the *line regulation*.

Theory Background

The fundamentals of LDO regulators are provided in this section *(see [1][4][11][12] for a general discussion of LDO regulators operation and characteristics, and [2] for more details on TPS7A4901 operation and features).*

Figure 2 shows the architecture of a low-dropout (LDO) regulator using a PNP bipolar transistor as pass device connected between the input and the output. The output voltage is sensed through the voltage divider R_{f1}-R_{f2}, that generates the feedback voltage V_{FB}. The Error Amplifier adjusts the pass device base current until the emitter-collector voltage V_{EC} equals the difference between the input voltage V_{in} and the desired regulated output voltage given by the formula (1):

(1) $$V_{OUT} = V_{ref}(1+R_{f1}/R_{f2})$$

where V_{ref} is the internal reference voltage. The base current I_B is injected into ground, and depends on the line and load conditions. The PNP transistor must work in the active region in order to achieve the output voltage V_{OUT} given by (1).

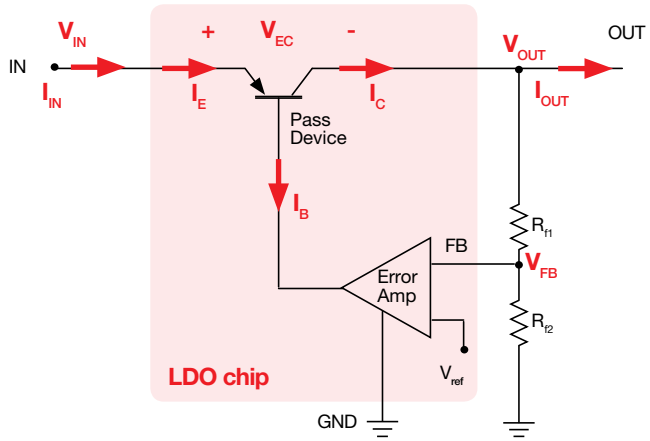


Figure 2

Figure 3 shows the output characteristic of a PNP bipolar transistor. The PNP transistor works in the active region, thus ensuring a regulated output voltage, provided that the input voltage V_{IN} is greater than $V_{INmin} = V_{OUT} + V_{EC,sat}(I_{OUT})$, where $V_{EC,sat}(I_{OUT})$ is the saturation emitter-collector voltage at the current I_{OUT} required by the load. The voltage V_{INmin} is called **dropout voltage**.

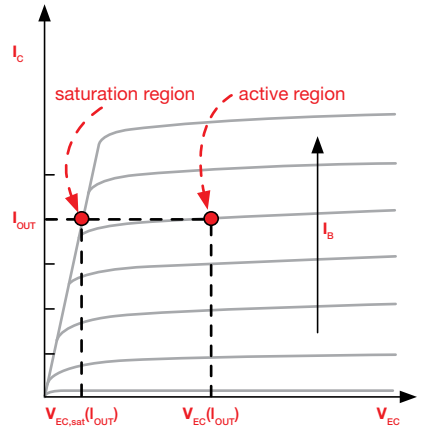


Figure 3

Figure 4 shows the effect of output voltage de-rating caused by the decrease of input voltage below V_{INmin}. When V_{IN} is lower than the **dropout voltage** V_{INmin}, the PNP transistor works in the saturation region of Figure 3, and is not able to deliver the current I_{OUT} required by the load. Therefore, the output voltage V_{OUT} is derated with respect to the desired nominal value V_{OUTnom}. This corresponds to the **dropout region** in Figure 4.

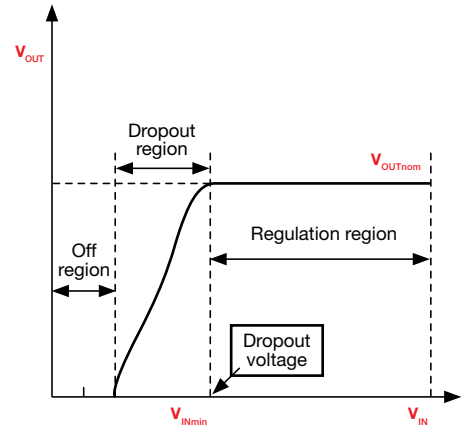


Figure 4

Good to Know

1. In theory, it is possible to find a ratio of resistances $R_{f1}/R_{f2} = V_{OUTnom}/V_{ref}-1$, that corresponds to the desired value of the nominal output voltage V_{OUTnom}. In practice, the values of commercial resistances are standardized, so that in most cases the nominal ratio R_{f1}/R_{f2} cannot be exactly achieved with the two resistors voltage divider made of R_{f1} and R_{f2}, so that the regulated V_{OUT} does not equal V_{OUTnom}.
2. Commercial resistors are available with different tolerances. Resistors with 0.1% tolerance ensure higher regulation accuracy, but they are more expensive than 1% tolerance resistors, which cause instead a degradation of the accuracy.
3. The reference voltage V_{ref} of the LDO is set inside the IC and can have a tolerance of 1% to 2%, which influences the value of the regulated output voltage V_{OUT}.

Experiment set-up: configuration

The instruments needed for this experiment are: a DC POWER SUPPLY, four MULTIMETERS and a DC ELECTRONIC LOAD. Figure 5 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

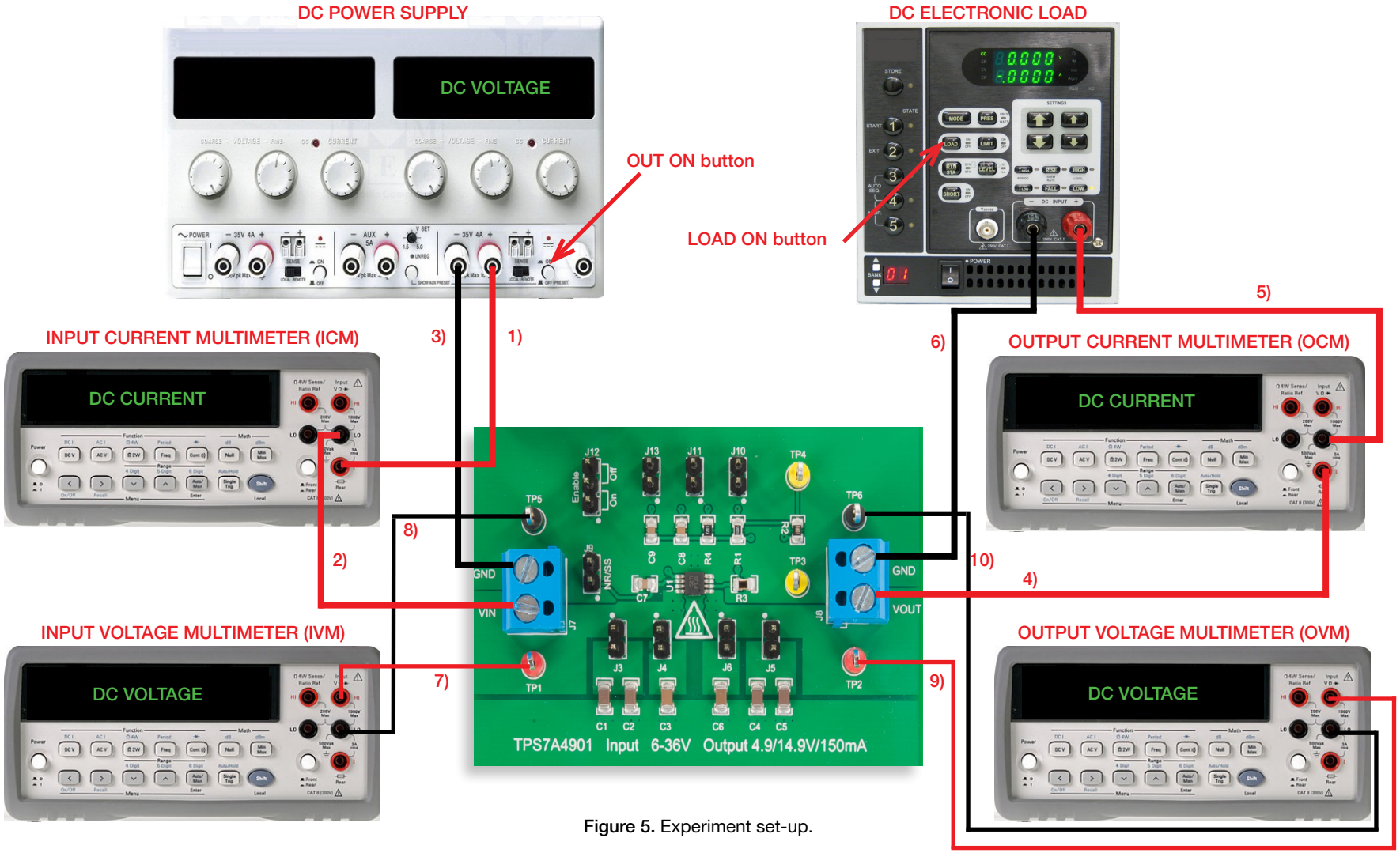


Figure 5. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the POSITIVE (RED) OUTPUT of the DC POWER SUPPLY to the POSITIVE (RED) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM)
[WARNING: the positive current input of the multimeter is distinguished from the positive voltage input]

2) connect the NEGATIVE (BLACK) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM) to the INPUT (VIN) of the J_7 screw terminal of the TPS7A4901 LDO regulator

3) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the GROUND (GND) of the J_7 screw terminal of the TPS7A4901 LDO regulator

4) connect the OUTPUT (VOUT) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the POSITIVE (RED) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM)
[WARNING: the positive current input of the multimeter is distinguished from the positive voltage input]

5) connect the NEGATIVE (BLACK) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM) to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD

6) connect the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD to the GROUND (GND) of the J_8 screw terminal of the TPS7A4901 LDO regulator

7) connect the POSITIVE (RED) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_1 which is the VIN of the TPS7A4901 LDO regulator

8) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_5 which is GND of the TPS7A4901 LDO regulator

9) connect the POSITIVE (RED) VOLTAGE INPUT of the OUPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_2 which is VOUT of the TPS7A4901 LDO regulator

10) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the OUTPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_6 which is the GND of the TPS7A4901 LDO regulator

Test#1: preparation and procedure

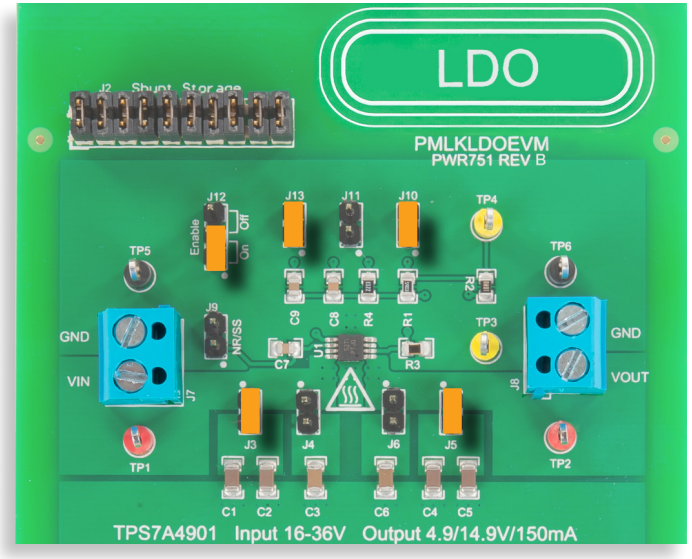


Figure 6. TPS7A4901 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 6):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7μF) and C_5 (4.7μF) output capacitors connected
- J_3 **shorted** → C_1 (4.7μF) and C_2 (4.7μF) input capacitors connected
- J_4 **open** → C_3 (2.2μF) input capacitor disconnected
- J_6 **open** → C_6 (2.2μF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤ 1A
3) set the OCM in DC CURRENT MODE, with range ≤ 1A
4) set the IVM in DC VOLTAGE MODE, with range ≥ 5V
5) set the OVM in DC VOLTAGE MODE, with range ≥ 5V
6) turn on the POWER SUPPLY (ensure that the “OUT ON” button is OFF)
7) set the VOLTAGE of the POWER SUPPLY at 6V
8) set the POWER SUPPLY CURRENT LIMIT at 200mA
9) turn on the ELECTRONIC LOAD (ensure that the “LOAD ON” button is OFF)
10) set the ELECTRONIC LOAD in CONSTANT CURRENT MODE and the DC current at 25mA
11) turn ON the POWER SUPPLY “OUT ON” button
12) in these conditions you should read about 6V in the IVM display, about 5V in the OVM display, about 0A in the OCM display and 0A in the ICM display (if you don’t read these values, turn OFF the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
13) turn ON the ELECTRONIC LOAD “LOAD ON” button
14) in these conditions you should read about 6V in the IVM display, about 5V in the OVM display, 25mA in the OCM display and slightly more than 25mA in the ICM display (if you read values much different than the one listed above, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
15) reduce slowly the DC POWER SUPPLY voltage by means of the “fine adjust” knob, watch the output voltage of the TPS7A4901 LDO regulator on the OVM display, stop when you see the voltage to decrease by more than 0.1%, and record the input voltage and the output voltage values in Table 1
16) reset the DC POWER SUPPLY voltage at 6V and repeat step 15) for the values of the load current listed in Table 1
17) turn OFF the ELECTRONIC LOAD “LOAD ON” button, turn OFF the DC POWER SUPPLY “OUT ON” button
18) open jumper J_{10} to set 15V nominal output voltage V_{out}, repeat the steps 10) to 16) by setting the initial value of VOLTAGE of the POWER SUPPLY at 16V (the values 6V and 5V now are 16V and 15V), and fill Table 1
19) at the end of the measurements, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

For each position of jumper J_{10} (open/shorted), execute the following steps.

1) Calculate the nominal output voltage [(a)] V_{outnom} based on the formula (1) provided in the *Theory Background* section, using the R_{f1} and R_{f2} values provided in the parameters box below, and report the value in Table 1 [**NOTE:** neglect the tolerances of the sensing resistors].
2) For the value of the load current of 25mA, measure the output voltage [(b)] $V_{out,1V}$ at $V_{IN}=V_{outnom}+1V$, and report the value in Table 1.
3) For each value of the load current of Table 1, measure the value of the input voltage [(1)] V_{inmin} at which you observe an output voltage value [(2)] $V_{out,0.1\%}$ deviating of more than 0.1% from the value measured at $V_{IN}=V_{outnom}+1V$ [e.g. 5mV at 5V], calculate the drop voltage [(3)] $V_{drop}= V_{inmin} - V_{out,0.1\%}$, and report the values V_{inmin}, $V_{out,0.1\%}$ and V_{drop} in Table 1.
4) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][4].

Table 1. Dropout voltage of TI-PMLK TPS7A4901 LDO regulator vs load corrent at V_{OUT} = 5V and V_{OUT} = 15V

	I_{OUT} [mA]	25	50	75	100	125	150
J_{10} shorted ($V_{outnom} \approx 5V$) [(a)] $V_{outnom} = V_{ref}(1+R_{f1@J10sh}/R_{f2})$ = ... V [(b)] $V_{out,1V}@\{V_{IN}=V_{outnom}+1V, I_{OUT}=25mA\}$ = ... V	(1) V_{INmin} [V]	(1)	(1)	(1)	(1)	(1)	(1)
	(2) $V_{OUT,0.1\%}$ [mV]	(2)	(2)	(2)	(2)	(2)	(2)
	(3) $V_{drop} = V_{INmin}$ - (2)$V_{OUT,0.1\%}$ [mV]	(3)	(3)	(3)	(3)	(3)	(3)
J_{10} open ($V_{outnom} \approx 15V$) [(a)] $V_{outnom} = V_{ref}(1+R_{f1@J10op}/R_{f2})$ = ... V [(b)] $V_{out,1V}@\{V_{IN}=V_{outnom}+1V, I_{OUT}=25mA\}$ = ... V	(1) V_{INmin} [V]	(1)	(1)	(1)	(1)	(1)	(1)
	(2) $V_{OUT,0.1\%}$ [mV]	(2)	(2)	(2)	(2)	(2)	(2)
	(3) $V_{drop} = V_{INmin}$ - (2)$V_{OUT,0.1\%}$ [mV]	(3)	(3)	(3)	(3)	(3)	(3)

Sensing resistors:

J_{10} open (V_{OUT} = 15V):
$R_{f1} = R_1 = 590k\Omega$, ±1.0% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

J_{10} shorted (V_{OUT} = 5V):
$R_{f1} = R_1(590k\Omega$, ±1.0% tolerance) in parallel to $R_4(221k\Omega$, 1.0% tolerance)
$= 160.8k\Omega$, ±0.5% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

TPS7A4901 reference voltage:
V_{ref}= 1.194V ±1.5% tolerance

Answer:

1. Does the dropout voltage increase or decrease with increasing load current? ☐ increases ☐ decreases ☐ other: _____

2. How does the dropout voltage change at different V_{out}? ☐ higher at 15V ☐ higher at 5V ☐ other: _____

Test#2: preparation and procedure

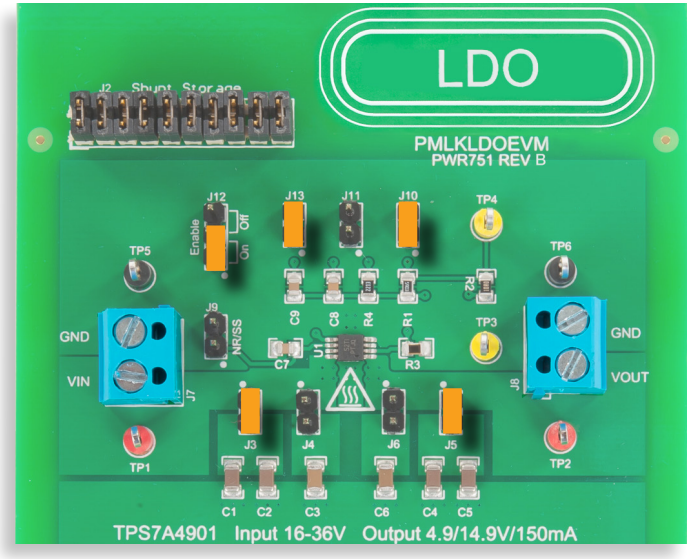


Figure 7. TPS7A4901 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 7):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7μF) and C_5 (4.7μF) output capacitors connected
- J_3 **shorted** → C_1 (4.7μF) and C_2 (4.7μF) input capacitors connected
- J_4 **open** → C_3 (2.2μF) input capacitor disconnected
- J_6 **open** → C_6 (2.2μF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤ 1A
3) set the OCM in DC CURRENT MODE, with range ≤ 1A
4) set the IVM in DC VOLTAGE MODE, with range ≥ 10V
5) set the OVM in DC VOLTAGE MODE, with range ≥ 20V
6) turn on the POWER SUPPLY (ensure that the “OUT ON” button is OFF)
7) set the VOLTAGE of the POWER SUPPLY at 6V
8) set the POWER SUPPLY CURRENT LIMIT at 200mA
9) turn on the ELECTRONIC LOAD (ensure that the “LOAD ON” button is OFF)
10) set the ELECTRONIC LOAD in CONSTANT CURRENT MODE and the DC current at 50mA
11) turn ON the POWER SUPPLY “OUT ON” button
12) in these conditions you should read about 6V in the IVM display, about 5V in the OVM display, about 0A in the OCM display and 0A in the ICM display (if you don’t read these values, turn OFF the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
13) turn ON the ELECTRONIC “LOAD ON” button
14) in these conditions you should read about 6V in the IVM display, about 5V in the OVM display, 50mA in the OCM display and slightly more than 50mA in the ICM display (if you read values much different than the ones listed above, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
15) read the output voltage on the OVM display, record the value in Table 2 and repeat this step for all the values of the load current listed in Table 2, by changing the ELECTRONIC LOAD DC current set point (you do not need to turn OFF the ELECTRONIC LOAD “LOAD ON” button). Adjust the POWER SUPPLY knob until you read 6V on the IVM display for each value of the load current
16) set the ELECTRONIC LOAD DC current at 50mA, read the output voltage on the OVM display, record the value in Table 3 and repeat this step for all the values of the input voltage listed in Table 3, by changing the POWER SUPPLY DC voltage set point (you do not need to turn OFF the POWER SUPPLY “OUT ON” button). Adjust the POWER SUPPLY knob until you read the desired input voltage on the IVM display for each value of the load current
17) at the end of the measurements, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) Calculate the nominal output voltage V_{out} based on the formula (1) provided in the *Theory Background* section, using the R_{f1} and R_{f2} values provided in the parameters box below.
2) With input voltage fixed at V_{in} = 6V, measure the value of the output voltage V_{out} for each value of the load current I_{out} and report the value in Table 2.
3) Calculate the percent LOAD REGULATION, by means of the formula $(V_{out}-V_{outnom})/V_{outnom}$x100, for each value of the load current I_{out} and report the value in Table 2.
4) With load current fixed at I_{out} = 50mA, measure the value of the output voltage V_{out} for each value of the input voltage V_{in} and report the value in Table 3.
5) Calculate the percent LINE REGULATION, by means of the formula $(V_{out}-V_{outnom})/V_{outnom}$x100, for each value of the input voltage V_{in} and report the value in Table 3.
6) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][4].

Table 2. Load regulation of TPS7A4901 LDO regulator at V_{OUT} = 5V

V_{IN} = 6V	I_{OUT} [mA]					
	25	50	75	100	125	150
V_{OUT} [V]						
load regulation [%]						

Table 3. Line regulation of TPS7A4901 LDO regulator at V_{OUT} = 5V

I_{OUT} = 50mA	V_{IN} [V]					
	6	9	12	15	18	21
V_{OUT} [V]						
line regulation [%]						

Sensing resistors:

J_{10} open (V_{OUT} = 15V):
$R_{f1} = R_1$ = 590kΩ, ±1.0% tolerance
$R_{f2} = R_3$ = 51.1kΩ, ±0.1% tolerance

J_{10} shorted (V_{OUT} = 5V):
$R_{f1} = R_1$(590kΩ, ±1.0% tolerance) in parallel to R_4(221kΩ, 1.0% tolerance)
= 160.8kΩ, ±0.5% tolerance
$R_{f2} = R_3$ = 51.1kΩ, ±0.1% tolerance

TPS7A4901 reference voltage:
V_{ref}= 1.194V±1.5% tolerance

Answer:

1. Does the output voltage increase with the load current? ☐ yes ☐ no ☐ it depends on: _____

2. Does the output voltage increase with the line voltage? ☐ yes ☐ no ☐ it depends on: _____

Discussion

In Test#1 we are interested in investigating correlations between the value of the *dropout voltage* and the values of the load current and of the input voltage.

The LDO dropout voltage increases as the output current increases, as shown in the plot of Figure 8. This is determined by the increase of the emitter-to-collector voltage of the bipolar PNP pass device operating in saturation, as the current passing through the device increases. An LDO regulator characterized by a lower dropout voltage is able to work with a smaller difference between the input voltage and the output voltage (see *Experiment 5* for dropout voltage discussion relevant to N-channel MOSFET LDO regulators). This has two main positive consequences: the regulation region is expanded and the maximum efficiency of the LDO regulator increases (see *Experiment 2* for efficiency analysis of LDO regulators).

In Test#2 we are interested in investigating correlations between the value of the output voltage and the values of the load current and of the input voltage.

The plots of line and load regulation of TPS7A4901 LDO regulator are shown in Figures 10 and 11. The line and load regulation are a measure of the steady-state tolerance of the LDO regulator. A smaller value of line regulation or load regulation means that the regulated output voltage is less sensitive to the input voltage or to the load current, respectively. In other words, the LDO regulator is able to neutralize the effects of input voltage and load current variations. Such ability is the result of various influence factors, such as the type and characteristics of the pass device, the type and characteristics of the operational amplifier used to realize the feedback error amplifier, the characteristics of the voltage reference generator, the characteristics of voltage divider resistors. For a given pass device, a high open-loop gain operational amplifier is the primary requisite to achieve good line/load regulation. The line regulation and load regulation contribute to the definition of the LDO regulator accuracy, which includes the cumulative effects of line/load regulation, reference voltage, op-amp, voltage divider resistors, and temperature (*see [2] for more details on thermal characteritics of TPS7A4901 LDO regulator and [12] for more details on the calculation of the LDO regulator accuracy*).

Experimental plots

The plots collected in the Figures 8 to 11 show the typical characteristics of TPS7A4901 LDO regulator (*see [2] for further details*).

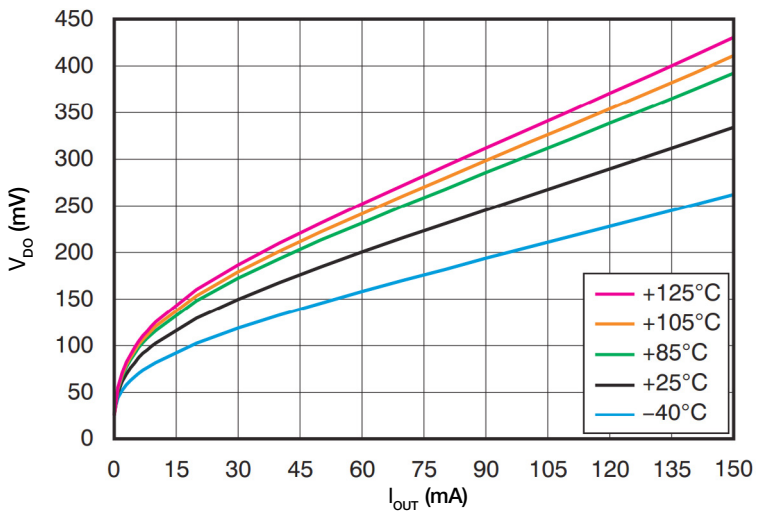


Figure 8. Dropout voltage of TPS7A4901 vs load current

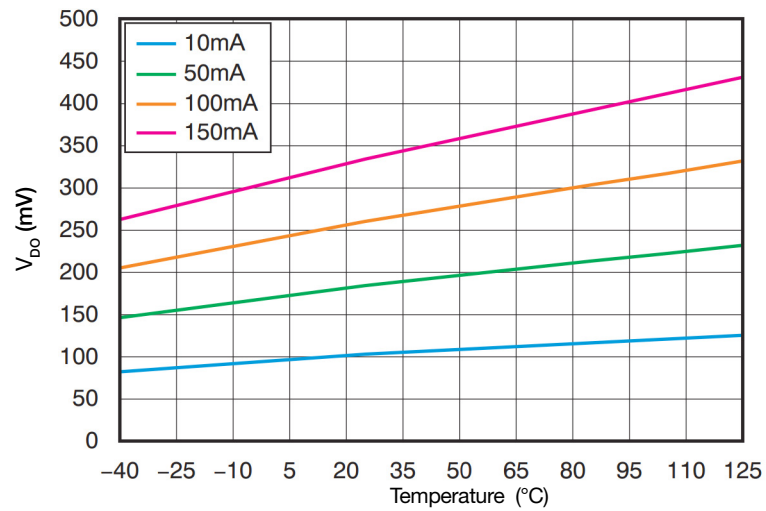


Figure 9. Dropout voltage of TPS7A4901 vs temperature

The dropout voltage also depends on the LDO chip junction temperature T_j. The plots of Figures 8 and 9 show how the droupout voltage of the TPS7A4901 LDO regulator changes with the junction temperature. The junction temperature, $T_j = T_a + R_{\theta ja} P_d$, depends on three main factors: the LDO chip power dissipation P_d determined by the current/voltage operating conditions, the ambient temperature T_a and the junction-to-ambient thermal resistance $R_{\theta ja}$ of the LDO regulator package (it is about $R_{\theta ja}$ = 55°C/W for TPS7A4901). Therefore, the measured dropout voltage changes with the ambient temperature (*see [2] for more details on thermal characteristics of TPS7A4901 LDO regulator and Experiment 2 for further insight in thermal analysis of* TPS7A4901 *LDO regulator*).

Experimental plots

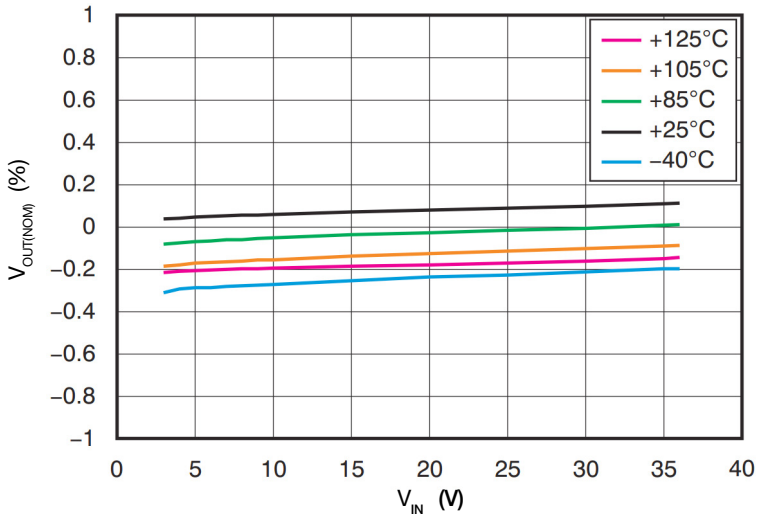


Figure 10. Line regulation of TPS7A4901, with temperature dependency

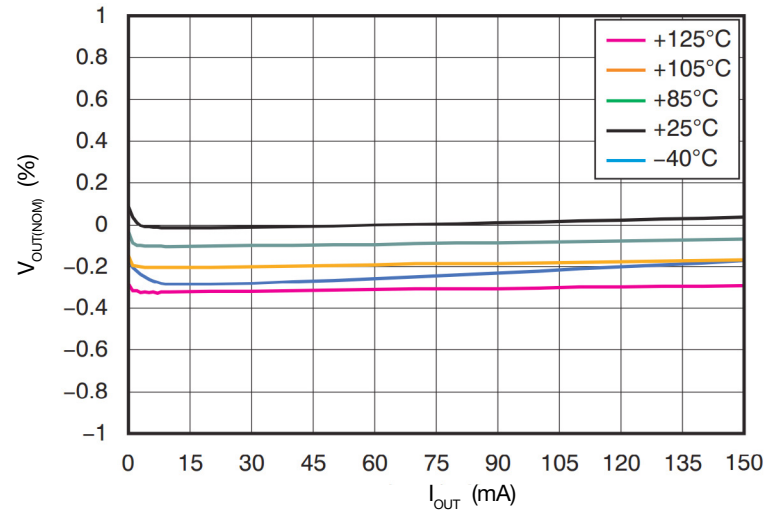


Figure 11. Load regulation of TPS7A4901, with temperature dependency

The plots of Figures 10 and 11 show the line regulation and load regulation of the TPS7A4901 LDO regulator, and their dependency on the LDO chip junction temperature. It can be observed that the both the line regulation and the load regulation are worse at very low temperature (below 0°C) and at very high temperature (above 100°C). The first situation is of interest in aerospace applications, where the ambient temperature is extremely low and the semiconductor devices inside the LDO regulator chip operate at a junction temperature below 0°C despite of their power dissipation. The second situation is of interest in automotive applications, if the LDO regulator is part of electronics located inside the engine compartment where the ambient temperature can be up to 80°C and more, or when the LDO regulator operates with a big difference between the input voltage V_{IN} and the output voltage V_{OUT}, which causes a high power dissipation inside the LDO regulator (*see [2] for more details on thermal characteristics of TPS7A4901 LDO regulator and Experiment 2 for further insight in efficiency analysis of* TPS7A4901 *LDO regulator*). It is interesting to note that in all the aforementioned situations, the line and load regulation become both negative. This means that the output voltage is always lower than the required nominal value. If a high accuracy is required by the specifications given for the application, it is possible to improve the line and load regulation by selecting a couple of resistors of the feedback voltage divider with appropriate values of resistances R_{f1} and R_{f2}, which allow to partially compensate the output voltage derating caused by the extreme temperature conditions. In other words, according to the formula (1) provided in the *Theory Background* section, the voltage divider can be designed so that the nominal output voltage is slightly higher than the nominal value, thus neutralizing the derating caused by the extreme temperature conditions. In order to make this solution really feasible, resistors with 0.01% to 0.1% tolerance are required, which may have some impact on the cost of the LDO solution.

Experiment 2

The goal of this experiment is to analyze how the efficiency of an LDO regulator depends on the line and load conditions. The TPS7A4901 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze the correlations between the efficiency of the LDO regulator and the values of the load current and of the input voltage.

The subject of investigation in this experiment is the efficiency of LDO regulators. Figure 1 shows the simplified schematic of the TPS7A4901 LDO regulator. The main contributors that affect the efficiency of LDO regulators are: the pass device, the LDO architecture and the operating conditions. The pass device of LDO regulators is characterized by power dissipation which increases when the difference between input voltage and output voltage increases. The LDO architecture influences the efficiency as it determines the ground current I_{gnd}, also called quiescent current, which is the difference between the LDO regulator input and output currents. The ground current I_{gnd} consists of several components, determined by the band-gap reference, the sensing resistors, the error amplifier, and the pass device drive current. The ground current and the voltage drop across the pass device are determined by the load current and input voltage operating conditions. LDO regulators efficiency calculation is discussed in detail in the *Theory Background* section.

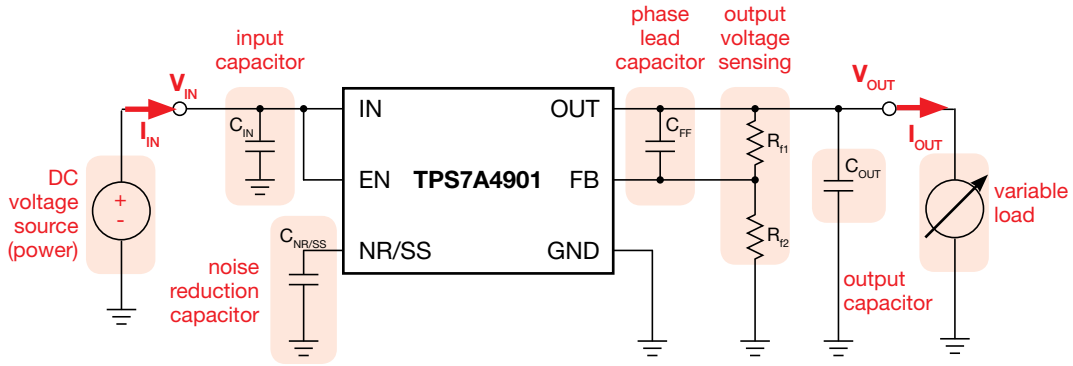


Figure 1. Simplified schematic of the TPS7A4901 LDO regulator

Test#1. We measure the input voltage V_{IN}, the input current I_{IN}, output voltage V_{OUT} and output current I_{OUT} of the TPS7A4901 LDO regulator while varying the load current. The goal is to evaluate the percent efficiency of the LDO regulator, and to observe if and how it depends on the load current. The test is repeated at different values of the input voltage to detect its influence on the efficiency.

Test#2. We measure the input voltage V_{IN}, the input current $I_{IN,}$ the output voltage V_{OUT} and output current I_{OUT} of the TPS7A4901 LDO regulator while varying the input voltage. The goal is to evaluate the percent efficiency of the LDO regulator, to observe if and how it depends on the input voltage and to compare the measured efficiency with the results of efficiency calculation realized by means of formulae provided in the *Theory Background* section, including a basic thermal analysis. The test is repeated at different values of the output current.

Theory Background

The fundamentals of LDO loss analysis are provided in this section *(see [1][4][12] for a general discussion of LDO regulators operation and characteristics, and [2] for more details on TPS7A4901 operation and features).*

Figure 2 shows an LDO regulator using a PNP bipolar transistor pass device. The pass device voltage V_{EC} equals the difference between the input voltage V_{IN} and the output voltage V_{OUT}. The total LDO regulator power dissipation is given by the formula (1):

$$(1) \quad P_d = P_{IN} - P_{OUT} = V_{IN} I_{IN} - V_{OUT} I_{OUT}$$

The dissipation is determined by the LDO chip and by the voltage divider resistors R_{f1} and R_{f2}. The LDO regulator input current fulfills the equation (2) :

$$(2) \quad I_{IN} = I_{OUT} + I_{GND} + I_{VD}$$

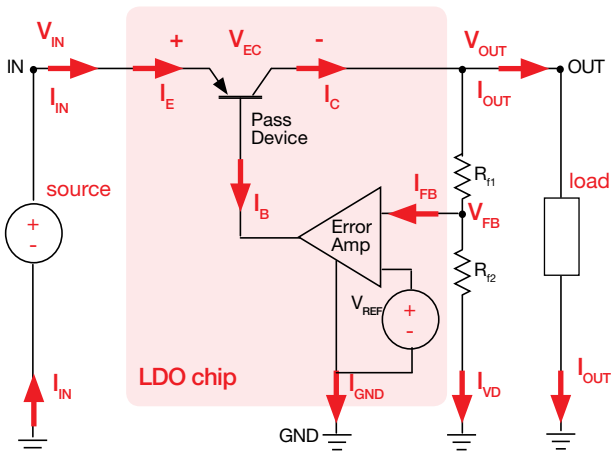


Figure 2

Based on formula (1), given the output voltage V_{OUT} and the output current I_{OUT}, the LDO regulator power dissipation increases if the input voltage increases. The PNP pass device is the main contributor to the power dissipation. Figure 3 shows the output characteristic of a PNP bipolar transistor. The output voltage regulation is ensured provided that the input voltage is higher than the *dropout voltage* (see *Experiment 1*). In this case, the PNP transistor operates in the active region and its voltage $V_{EC}(I_{OUT}) = V_{IN} - V_{OUT}$ is higher than the saturation voltage $V_{EC,sat}(I_{OUT})$.

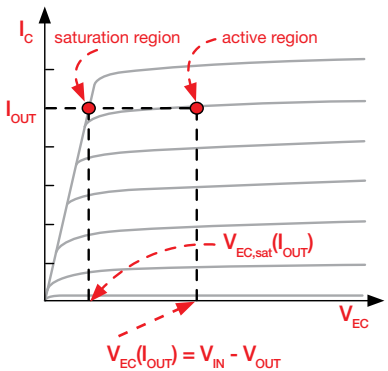


Figure 3

The LDO regulator efficiency η is given by the formula (3):

$$(3) \quad \eta = P_{OUT} / P_{IN} = V_{OUT} I_{OUT} / [V_{IN} (I_{OUT} + I_{GND} + I_{VD})] \times 100$$

where $I_{VD} = V_{ref}/R_{F2}$ and the I_{GND} depends on LDO input voltage V_{IN}, load current I_{OUT} and junction temperature T_j, as shown in Figure 4. The LDO junction temperature T_j depends in turn on the LDO chip power losses P_{LDO} according to formula (4):

$$(4) \quad T_j = T_a + R_{\theta ja} P_{LDO}$$

where $R_{\theta JA}$ is the LDO chip thermal resistance, T_a is the ambient temperature and:

$$(5) \quad P_{LDO} = V_{IN} I_{IN} - V_{OUT} I_{OUT} - (R_{f1} + R_{f2}) I_{VD}^2$$

The LDO ground current I_{GND} depends on the base current needed to bias the pass device, on the error amplifier op-amp, on the voltage reference and on the junction temperature. Figure 4 shows the ground current vs output current and input voltage for the TPS7A4901 LDO regulator.

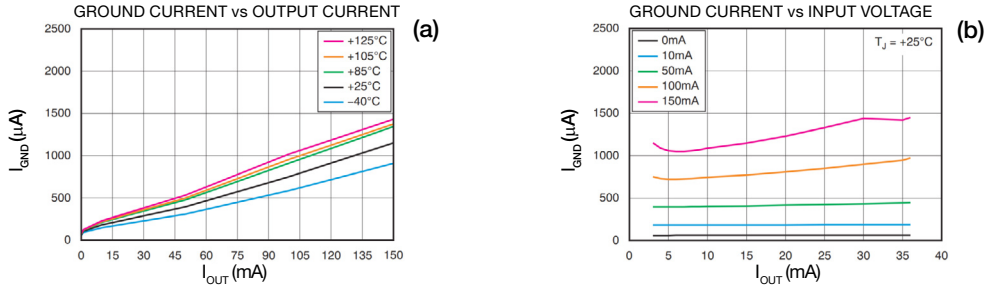


Figure 4

Good to Know

The LDO regulator sinks a quiescent current I_Q from the line, even when it is not delivering current to the load (*see [1][2][12] for details*).

Experiment set-up: configuration

The instruments needed for this experiment are: a DC POWER SUPPLY, four MULTIMETERS and a DC ELECTRONIC LOAD. Figure 5 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

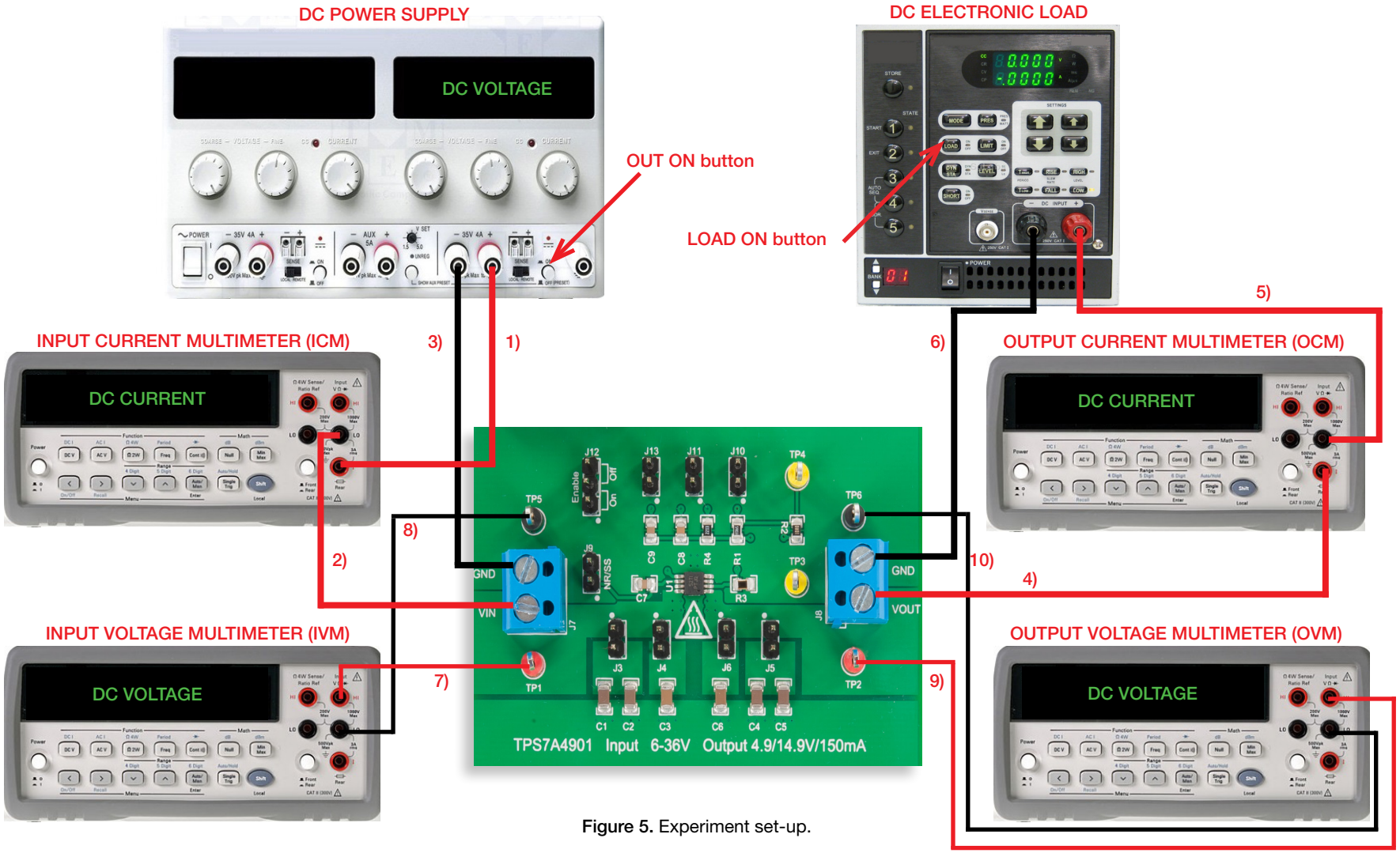


Figure 5. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the POSITIVE (RED) OUTPUT of the DC POWER SUPPLY to the POSITIVE (RED) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM)
[WARNING: the positive current input of the multimeter is distinguished from the positive voltage input]

2) connect the NEGATIVE (BLACK) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM) to the INPUT (VIN) of the J_7 screw terminal of the TPS7A4901 LDO regulator

3) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the GROUND (GND) of the J_7 screw terminal of the TPS7A4901 LDO regulator

4) connect the OUTPUT (VOUT) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the POSITIVE (RED) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM)
[WARNING: the positive current input of the multimeter is distinguished from the positive voltage input]

5) connect the NEGATIVE (BLACK) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM) to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD

6) connect the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD to the GROUND (GND) of the J_8 screw terminal of the TPS7A4901 LDO regulator

7) connect the POSITIVE (RED) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_1 which is the VIN of the TPS7A4901 LDO regulator

8) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_5 which is GND of the TPS7A4901 LDO regulator

9) connect the POSITIVE (RED) VOLTAGE INPUT of the OUPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_2 which is VOUT of the TPS7A4901 LDO regulator

10) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the OUTPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_6 which is the GND of the TPS7A4901 LDO regulator

Test#1: preparation and procedure

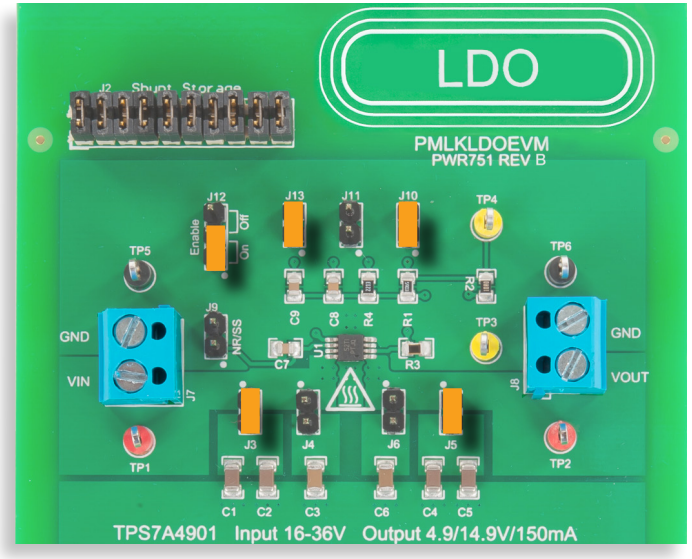


Figure 6. TPS7A4901 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 6):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7μF) and C_5 (4.7μF) output capacitors connected
- J_3 **shorted** → C_1 (4.7μF) and C_2 (4.7μF) input capacitors connected
- J_4 **open** → C_3 (2.2μF) input capacitor disconnected
- J_6 **open** → C_6 (2.2μF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤ 1A
3) set the OCM in DC CURRENT MODE, with range ≤ 1A
4) set the IVM in DC VOLTAGE MODE, with range ≥ 5V
5) set the OVM in DC VOLTAGE MODE, with range ≥ 5V
6) turn on the POWER SUPPLY (ensure that the “OUT ON” button is OFF)
7) set the VOLTAGE of the POWER SUPPLY at 8V
8) set the POWER SUPPLY CURRENT LIMIT at 200mA
9) turn on the ELECTRONIC LOAD (ensure that the “LOAD ON” button is OFF)
10) set the ELECTRONIC LOAD in CONSTANT CURRENT MODE and the DC current at 25mA
11) turn ON the POWER SUPPLY “OUT ON” button
12) in these conditions you should read about 8V in the IVM display, 5V in the OVM display, 0A in the OCM display and 0A in the ICM display (if you don’t read these values, turn OFF the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps). Adjust the POWER SUPPLY knob until you read 8V on the IVM display
13) turn ON the ELECTRONIC LOAD “LOAD ON” button
14) in these conditions you should read about 8V in the IVM display, about 5V in the OVM display, 25mA in the OCM display and slightly more than 25mA in the ICM display (if you read values much different than the one listed above, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
15) read the output voltage and the input current of the TPS7A4901 LDO regulator on the OVM display and ICM display respectively, record the output voltage and the input current values in Table 1, and repeat this step for all the values of the load current listed in Table 1 (Adjust the POWER SUPPLY knob until you read 8V on the IVM display for each value of the load current)
16) change the POWER SUPPLY DC voltage set point to 10V (you do not need to turn OFF the POWER SUPPLY “OUT ON” button), and repeat the step 15)
17) at the end of the measurements, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

1) For each value of the nominal input voltage and of the nominal load current indicated in Table 1, measure the input voltage V_{IN}, the input current I_{IN}, the output voltage V_{OUT}, the output current I_{OUT}, and collect the results in Table 1. [NOTE: the measured input voltage and the measured output current are the values that you read on the IVM and OCM MULTIMETERS: they might not be exactly equal to the the nominal input voltage and the nominal output current indicated in Table 1 due to resolution of the DC POWER SUPPLY and of the DC ELECTRONIC LOAD; in each measurement adjust the DC POWER SUPPLY and the DC ELECTRONIC LOAD set points so as the values you read in the IVM and OCM MULTIMETERS are as close as possible to the nominalinput voltage and the nominal output current indicated in Table 1].
2) Calculate the percent efficiency by means of the formula $\eta = V_{OUT}\, I_{OUT} / (V_{IN}\, I_{IN}) \times 100$ and report the result in Table 1.
3) Analyze the measurement results, answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][4].

Table 1. Efficiency of TI-PMLK TPS7A4901 LDO regulator vs load corrent, at output voltage V_{OUT} = 5V.

(1) V_{IN} [V] (2) I_{IN} [mA] (3) V_{OUT} [V] (4) I_{OUT} [mA] (5) η [%]	I_{OUT} [mA]											
	25		50		75		100		125		150	
V_{IN} = 8V	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)
	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)
	(5)		(5)		(5)		(5)		(5)		(5)	
V_{IN} = 10V	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)
	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)
	(5)		(5)		(5)		(5)		(5)		(5)	

Sensing resistors:

J_{10} open (V_{OUT} = 15V):
$R_{f1} = R_1 = 590k\Omega$, ±1.0% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

J_{10} shorted (V_{OUT} = 5V):
$R_{f1} = R_1(590k\Omega$, ±1.0% tolerance) in parallel to $R_4(221k\Omega$, 1.0% tolerance)
$= 160.8k\Omega$, ±0.5% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

TPS7A4901 reference voltage:
V_{ref}= 1.194V ±1.5% tolerance

Answer:

1. Does the line current equal the load current? ☐ yes ☐ no ☐ it depends on: _____

2. Which operating parameter has the greatest influence on the efficiency? ☐ the line voltage ☐ the load current ☐ it depends on: _____

Test#2: preparation and procedure

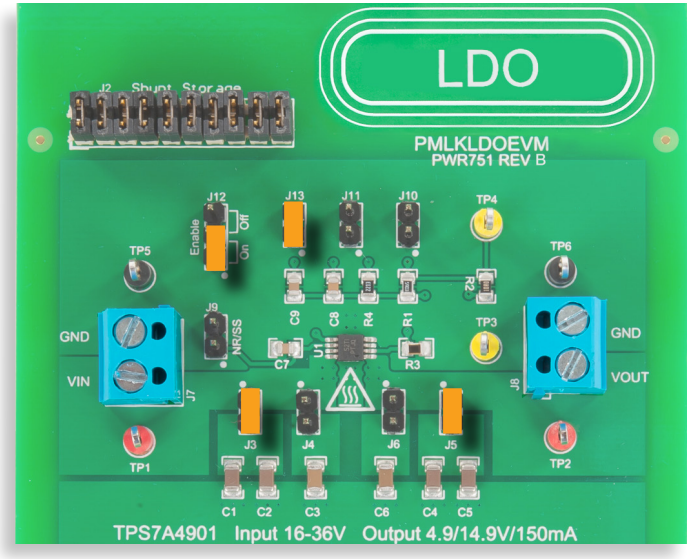


Figure 7. TPS7A4901 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 7):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **open** → nominal output voltage V_{out} = 15V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7µF) and C_5 (4.7µF) output capacitors connected
- J_3 **shorted** → C_1 (4.7µF) and C_2 (4.7µF) input capacitors connected
- J_4 **open** → C_3 (2.2µF) input capacitor disconnected
- J_6 **open** → C_6 (2.2µF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤ 1A
3) set the OCM in DC CURRENT MODE, with range ≤ 1A
4) set the IVM in DC VOLTAGE MODE, with range ≥ 15V
5) set the OVM in DC VOLTAGE MODE, with range ≥ 30V
6) turn on the POWER SUPPLY (ensure that the “OUT ON” button is OFF)
7) set the VOLTAGE of the POWER SUPPLY at 16V
8) set the POWER SUPPLY CURRENT LIMIT at 200mA
9) turn on the ELECTRONIC LOAD (ensure that the “LOAD ON” button is OFF)
10) set the ELECTRONIC LOAD in CONSTANT CURRENT MODE and set the DC current at 10mA
11) turn ON the POWER SUPPLY “OUT ON” button
12) in these conditions you should read about 16V in the IVM display, 15V in the OVM display, 0A in the OCM display and 0A in the ICM display (if you don’t read these values, turn OFF the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps). Adjust the POWER SUPPLY knob until you read 16V on the IVM display
13) turn ON the ELECTRONIC “LOAD ON” button
14) in these conditions you should read about 16V in the IVM display, about 15V in the OVM display, 10mA in the OCM display and slightly more than 25mA in the ICM display (if you read values much different than the one listed above, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
15) read the output voltage and the input current of the TPS7A4901 LDO regulator on the OVM display and ICM display respectively, use the values for the calculations required in Table 2, and repeat this step for all the values of the input voltage listed in Table 2 (adjust the POWER SUPPLY knob until you read the desired input voltage value on the IVM display)
16) change the ELECTRONIC LOAD DC current set point to 50mA (you do not need to turn OFF the ELECTRONIC LOAD “LOAD ON” button), and repeat the step 15
17) at the end of the measurements, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) For each value of the input voltage and of the load current indicated in Table 2, measure the input current I_{IN} and the output voltage V_{OUT}, calculate the experimental percent efficiency by means of the formula η_{exp} [%] = $V_{OUT}\ I_{OUT}$ / ($V_{IN}\ I_{IN}$) x 100 and report the result in Table 2.
2) Calculate the theoretical percent efficiency by means of the formula (3) provided in the *Theory Background* section and report the result in Table 2 [**NOTE:** use the plots of Figure 4(b) to determine the ground current I_{GND} of TPS7A4901 LDO regulator].
3) Calculate the LDO power losses P_{LDO} by means of the formula (5) provided in the *Theory Background* section, calculate the LDO chip junction temperature T_j by means of the formula (4) provided in the *Theory Background* section and report the result in Table 2 [**NOTE:** assume that the ambient temperature T_a is 25°C, or use a value of the ambient temperature measured nearby the LDO chip, if available].
4) Use the plots of Figure 4(a) to update the value of the ground current I_{GND}, based on the calculated junction temperature T_j, and to refine the value of the theoretical efficiency η_{theo} [%] calculated at point 2).
5) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][4].

Table 2. Experimental vs theoretical efficiency of TI-PMLK TPS7A4901 LDO regulator vs input voltage, at output voltage V_{OUT} = 15V

(1) exp η_{exp} [%]	(2) theo η_{theo} [%]	V_{IN}											
(3) loss P_d [mW]	(4) temp T_j [°C]	16V		18V		20V		22V		24V		26V	
I_{OUT} = 10mA		(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)
		(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)
I_{OUT} = 50mA		(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)	(1)	(2)
		(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)	(3)	(4)

Sensing resistors:

J_{10} open (V_{OUT} = 15V):
$R_{f1} = R_1 = 590k\Omega$, ±1.0% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

J_{10} shorted (V_{OUT} = 5V):
$R_{f1} = R_1(590k\Omega$, ±1.0% tolerance) in parallel to $R_4(221k\Omega$, 1.0% tolerance)
$= 160.8k\Omega$, ±0.5% tolerance
$R_{f2} = R_3 = 51.1k\Omega$, ±0.1% tolerance

TPS7A4901 reference voltage:
V_{ref}= 1.194V ±1.5% tolerance

Answer:

1. Which is the factors causing the main degradation of the LDO efficiency? ☐ the V_{IN}/V_{OUT} ratio ☐ the ground current I_{GND} ☐ the feedback current I_{FB}
☐ other : _____

2. Which are the input voltage and output current conditions allowing to achieve the maximum efficiency? _____

Discussion

In Test#1 we are interested in investigating correlations between the efficiency of the LDO regulator and the values of the load current.

Both the input voltage V_{IN} and the load current I_{OUT} have an impact on the LDO regulator efficiency. However, you may observe from experimental measurements that the input voltage V_{IN} has a much higher influence on the efficiency than the output current I_{OUT}. In fact, given the LDO regulator output voltage V_{OUT} and load current I_{OUT}, an increase of the input voltage V_{IN} directly translates into an increase of the pass device voltage V_{EC}, thus having a strong impact on the difference between the input power P_{IN} and the output power P_{OUT} of the LDO regulator, as highlighted in the formula (1) provided in the *Theory Background* section. Instead, given the LDO regulator output voltage V_{OUT} and input voltage V_{IN}, an increase of the load current I_{OUT} directly translates into an increase of the input current I_{IN} too, thus making the effect on the power losses limited to the increase of the LDO chip ground current I_{GND}, as highlihted in the formula (2) provided in the *Theoy Background* section. (*see Experiment 5 for ground current discussion relevant to N-channel MOSFET LDO regulators*).

In Test#2 we are interested in investigating correlations between the efficiency of the LDO regulator and the values of the input voltage, taking into accout the thermal properties of the LDO regulator.

The results of measurements should highlight that the main factor of influence on the efficiency is the ratio between the input voltage V_{IN} and the output voltage V_{OUT}, whereas the LDO chip ground current I_{GND} has minor influence, for the same reasons relevant to Test#1 discussed above. It should be noted that the ground current I_{GND} increases with the LDO chip junction temperature T_j, which in turn is higher when the input voltage V_{IN} is higher, due to the higher LDO losses P_{LDO}. Therefore, the increase of the input voltage V_{IN} boosts the ground current I_{GND}, thus having a two fold influence on the degradation of the effciency (*see [2] for more details on thermal characteritics of TPS7A4901 LDO regulator*).

Experimental plots

The plots collected in the Figures 8 to 11 show the typical characteristics of TPS7A4901 LDO regulator (*see [2] for further details*).

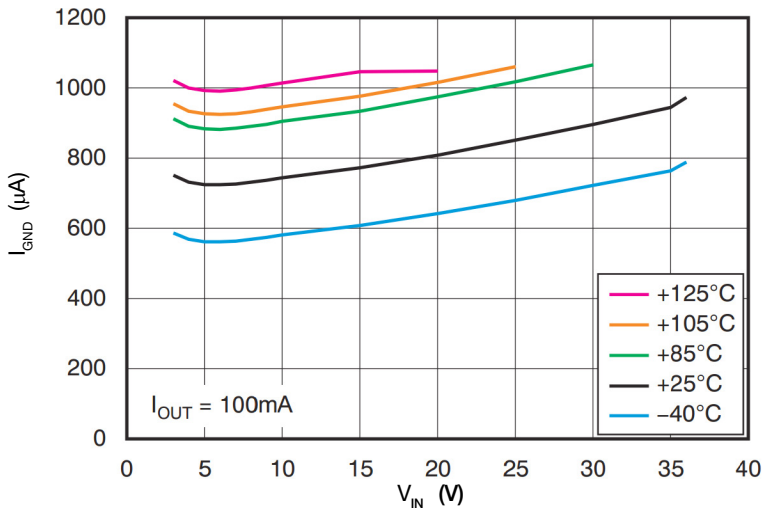


Figure 8. Ground current of TPS7A4901 LDO regulator vs input voltage at 100mA

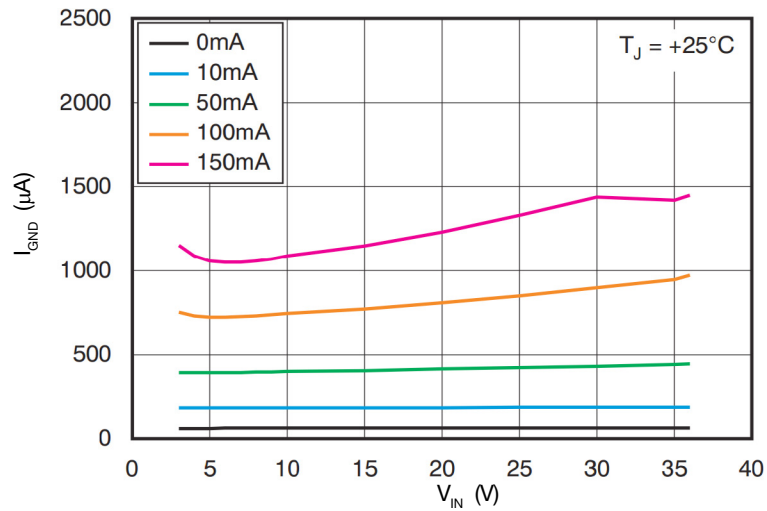


Figure 9. Ground current of TPS7A4901 LDO regulator vs input voltage at 25°C

The plots of Figures 8 and 9 provide a synoptic view of how the LDO chip ground current I_{GND} depends on input voltage V_{IN}, load current I_{OUT}, and junction temperature T_j. The voltage divider current I_{VD} has a very little influence on the efficiency, provided that its value is very small, as in the case of the TPS7A4901 LDO regulator. The voltage divider current I_{VD} depends on the LDO chip voltage reference V_{ref} and on the resistance R_{f2} of the output voltage divider, as shown in the *Theory Background* section.

Experimental plots

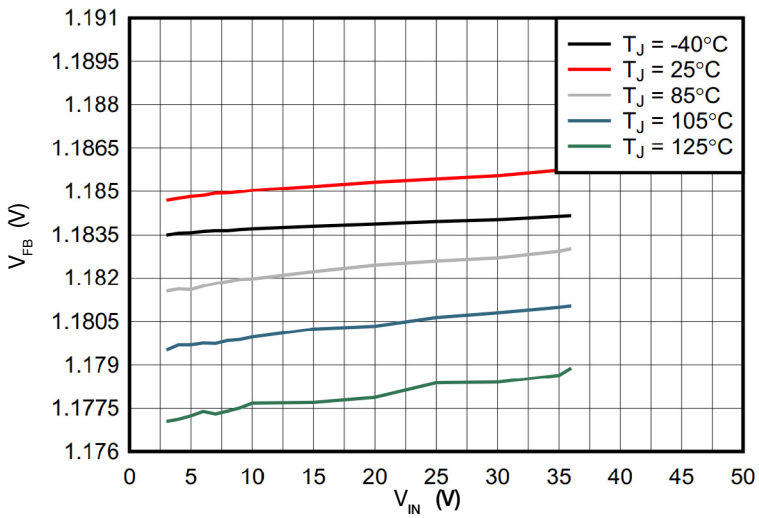


Figure 10. Feedback pin voltage of TPS7A4901 LDO regulator vs input voltage

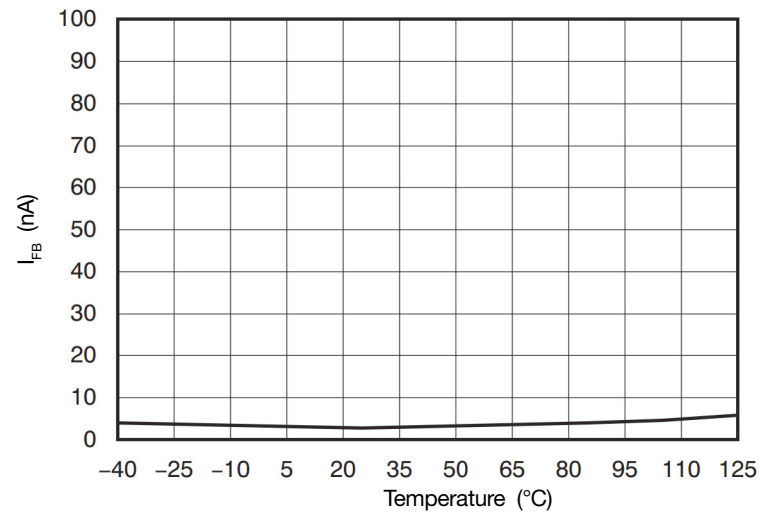


Figure 11. Feedback pin current of TPS7A4901 LDO regulator vs temperature

Figure 10 shows that the TPS7A4901 LDO regulator reference voltage has a little dependency with respect to the temperature, typical of a band gap voltage reference, and very little dependency with respect to the input voltage V_{IN}. As shown in the *Theory Background* section, the voltage divider current I_{VD} is set by the ratio V_{ref}/R_{f2}. The value of resistance R_{f2} cannot be too small as it can degrade the LDO efficiency (*see formula* (3)). At the same time, the value of resistance R_{f2} cannot be too high so as to make the voltage divider current I_{VD} comparable to the feedback current I_{FB} of the LDO feedback error amplifier: in this case, the resistors R_{f1} and R_{f2} would no longer work as a voltage divider and lead to degradation of the output voltage accuracy. Figure 11 shows the plot of the TPS7A4901 LDO regulator feedback current. In order to ensure that the resistors R_{f1} and R_{f2} operate like a voltage divider, the current I_{VD} has to be two to three orders of magnitude greater than the feedback current. For example, assuming I_{FB}=5nA and a factor I_{VD}/I_{FB}=500, we have I_{VD}=25mA and $R_{f2}=V_{ref}/I_{VD}$=48kΩ.

Experiment 3

The goal of this experiment is to analyze the LDO regulator stability and to investigate the effect of the output capacitor on load-transient and line-transient response. The TPS7A4901 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze the LDO regulator output voltage waveform in presence of load-transients, and to verify the stability.

The subject of investigation in this experiment is the stability for the LDO regulator. The condition shown in Figure 1 will be considered, where the TPS7A4901 LDO regulator is fed by a dyamic voltage source and terminated into a dynamic load. The LDO regulator must guarantee a good output voltage regulation in permanent steady-state conditions (*see Experiment 1 and Experiment 2*) and in the presence of line voltage and load current perturbations, which are frequent in many real world applications and may have different characteristics. For example, source voltage perturbations often occur in automotive power management, whereas load perturbations are commonly seen in systems using power amplifiers and logic devices. Perturbations involving fast variations of big magnitude are classified as line-transients and load-transients, whereas perturbations that are permanent, with moderate magnitude, and perhaps with some dominant harmonic spectrum, are classified as line-noise and load-noise.

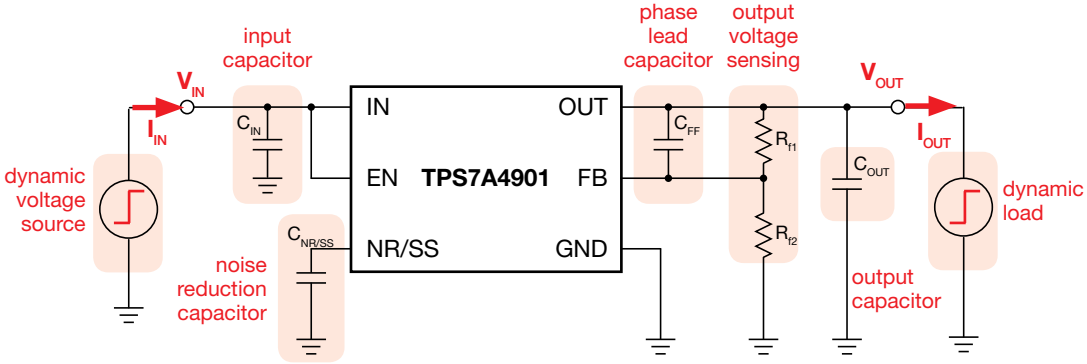


Figure 1. Simplified schematic of the TPS7A4901 LDO regulator

Test#1. We set-up the TPS7A4901 LDO regulator with a constant voltage source and record the output voltage waveform as the load current swings between two fixed levels. The expectation is that, after each load change, the output voltage has some small and short transient surge and then it returns close to the nominal value. The magnitude of the output voltage transient surges will be measured. The influence of the output capacitance C_{OUT} on the magnitude of voltage transient surges will be observed and discussed.

Test#2. We set-up the TPS7A4901 LDO regulator with a fixed load and apply a voltage source that swings between two fixed levels. The expectation is that, like in the load-transient case, after each input voltage change the output voltage has some transient surge and then it returns close to the nominal value. The magnitude of the output voltage transient surges will be measured. The influence of the output capacitance C_{OUT} on the magnitude of voltage transient surges will be observed and discussed.

Theory Background

The fundamentals of LDO regulators feedback compensation are provided in this section *(see [1][4][12] for a general discussion of LDO regulators operation and characteristics, and [2] for more details on TPS7A4901 operation and features).*

Figure 1 shows an LDO regulator with PNP bipolar transistor pass device.

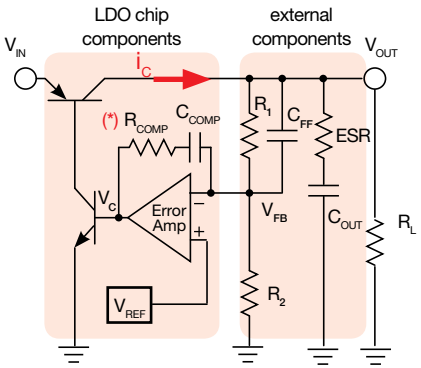


Figure 1

(*) The resistor R_{COMP} is typically used in LDOs designed to work with ceramic output capacitors.

The LDO regulates the output voltage by means of a feedback error amplifier, which compares the feedback voltage V_{FB} to a fixed reference voltage V_{REF} and changes the PNP pass transistor current as required by the load. Resistors R_1 and R_2 provide the voltage feedback to the error amplifier and set the reference-to-output gain $G_{VREF}=(1+R_1/R_2)$ which provides the output voltage $V_{OUT}=G_{VREF}V_{REF}$.

[NOTE: the LDO works ideally as a voltage-controlled voltage-source].

When the LDO voltage regulator of Figure 1 is stable it regulates the output voltage at the desired nominal value despite of input voltage and load current variations. The stability depends on the characteristics of the voltage feedback loop, highlighted in red in the block diagram of Figure 2. In particular, the stability is determined by the properties of the Voltage-Loop Gain (VLG) $T= G_{VC}G_{EA}$, where G_{VC} is the LDO control-to-output gain and G_{EA} is the error-amplifier gain.

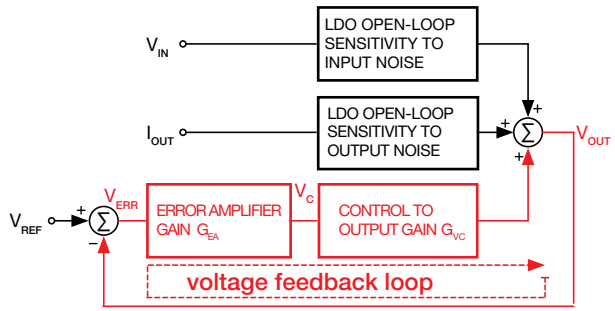


Figure 2

Figure 3 shows a VLG Bode plot. For robust stability, the phase margin ϕ_m has to be about 50° at the cross-over frequency ω_c, which is the frequency where the magnitude equals 0dB, and the phase shift ϕ_s (the shift between the minimum of the phase and -180°) has to be at least 20° in the frequency range below the cross-over frequency ω_c, where the magnitude is greater than 0dB.

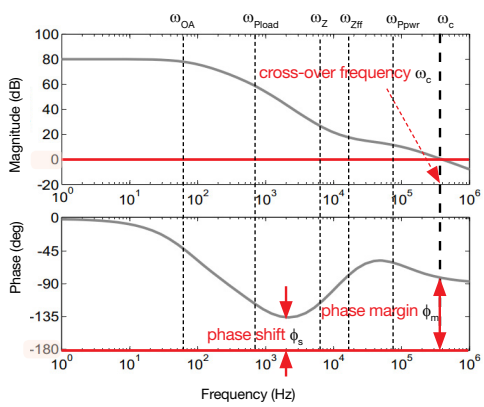


Figure 3

The G_{VC} and G_{EA} gains depend on LDO chip internal components (pass device, gate driver, op-amp, error amplifier feedback R_{COMP}-C_{COMP}), on external R-C components (R_{f1}, R_{f2}, C_{FF}, C_{OUT}, ESR) and on load current I_{OUT}. The resulting loop gain is given by equation (1):

$$T=T_0\frac{\left[1+\frac{s}{\omega_Z}\right]\left[1+\frac{s}{\omega_{Zff}}\right]}{\left[1+\frac{s}{\omega_{Pload}}\right]\left[1+\frac{s}{\omega_{Ppwr}}\right]\left[1+\frac{s}{\omega_{OA}}\right]} \quad (1)$$

$$\omega_{Pload}=\frac{I_{OUT}}{C_{OUT}V_{OUT}} \qquad \omega_Z=\begin{cases}\dfrac{1}{C_{OUT}ESR} & \text{(no } R_{COMP}\text{)}\\[2ex] \dfrac{1}{C_{COMP}R_{COMP}} & \text{(no ESR)}\end{cases}$$

$$\omega_{Zff}=\frac{1}{C_{FF}R_{f1}}$$

The phase lead of ω_Z zero improves the stability, provided that its frequency is neither too low nor too high. LDOs designed to work with ceramic output capacitors, having very low ESR, may include the resistance R_{COMP}, which combines with the capacitance C_{COMP} to generate the zero ω_Z. In principle, the capacitor C_{COMP} should introduce a pole in the origin. However, the finite DC gain of the op-amp limits the dc loop gain T_0, which is also influenced by the base-collector current gains of pass and gate drive devices, and introduces the pole ω_{OA}. The external capacitance C_{ff} introduces the zero ω_{Zff} which can be used to adjust the crossover frequency and phase margin. The high frequency pole ω_{Ppwr} depends on the capacitance of pass PNP device. The w_{Pload} pole depends on the load. While ω_{Pload}, ω_{Zff} and ω_Z (when determined by ESR) can be fixed by the LDO chip user, ω_{OA} and ω_{Ppwr} depend on LDO chip design and they are not disclosed in the datasheets.

Experiment set-up: configuration

The instruments needed for this experiment are: a POWER SUPPLY with DC and DYNAMIC MODE options, an ELECTRONIC LOAD with DC and DYNAMIC MODE options, and an OSCILLOSCOPE. Figure 5 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

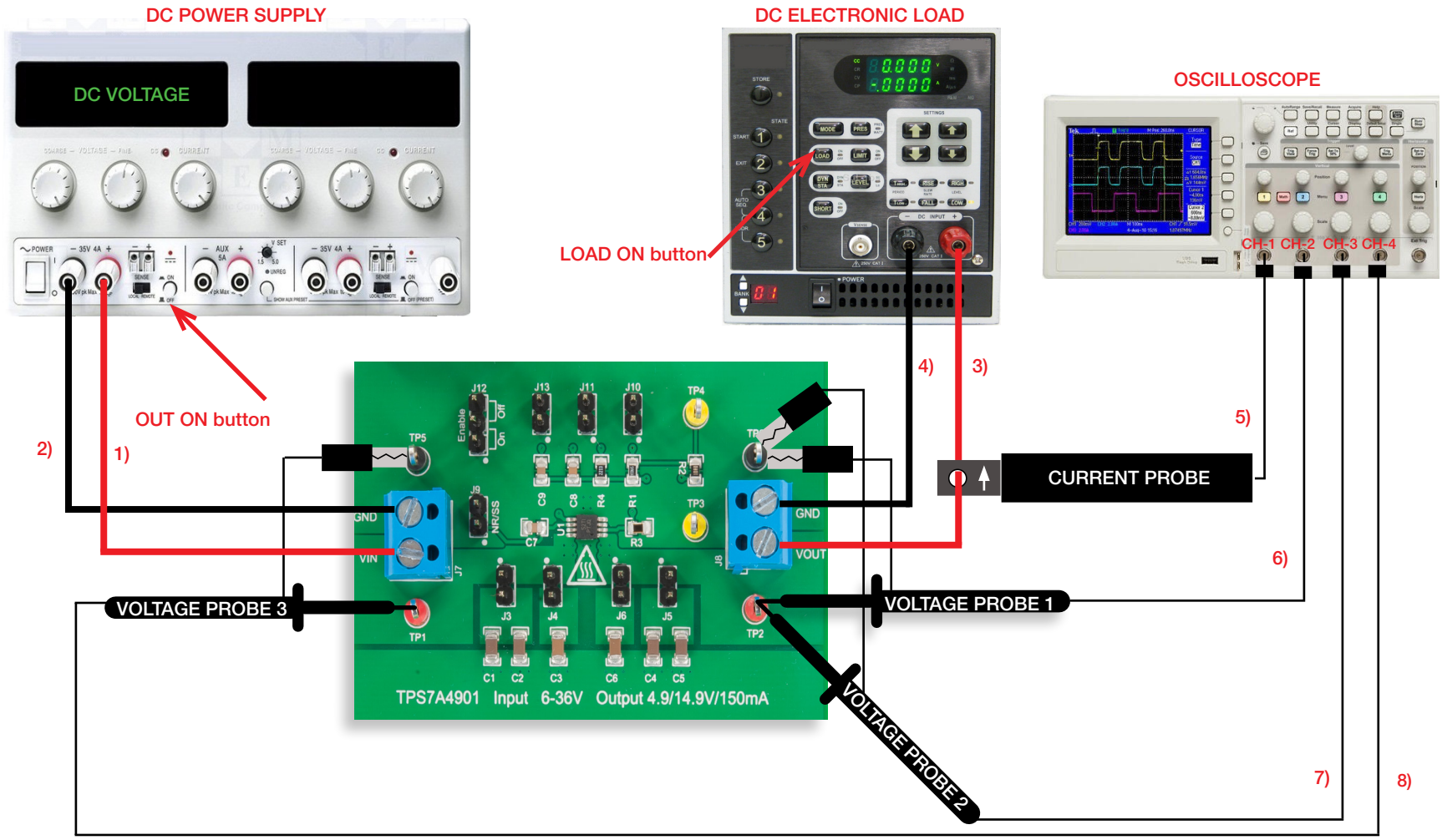


Figure 5. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the POSITIVE (RED) OUTPUT of the DC POWER SUPPLY to the INPUT (VIN) of the J_7 screw terminal of the TPS7A4901 LDO regulator

2) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the GROUND (GND) of the J_7 screw terminal of the TPS7A4901 LDO regulator

3) connect the OUTPUT (VOUT) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD

4) connect the GROUND (GND) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD

5) connect a current probe to channel 1 of the OSCILLOSCOPE and hang it on the cable connecting the OUTPUT (VOUT) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD, ensuring that the arrow printed on the probe clamps corresponds to the current that enters the ELECTRONIC LOAD.

6) connect a voltage probe to channel 2 of the OSCILLOSCOPE, hang its positive tip to TEST PIN TP_2 which is the output voltage of the TPS7A4901 LDO regulator. This probe will be used to measure the DC+AC components of the output voltage
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

7) connect a voltage probe to channel 3 of the OSCILLOSCOPE, hang its positive tip to TEST PIN TP_2 which is the output voltage of the TPS7A4901 LDO regulator. This probe will be used to measure the AC component of the output voltage
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

8) connect a voltage probe to channel 4 of the OSCILLOSCOPE, hang its positive tip to TEST PIN TP_1 which is the input voltage of the TPS7A4901 LDO regulator
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

Test#1: preparation and procedure

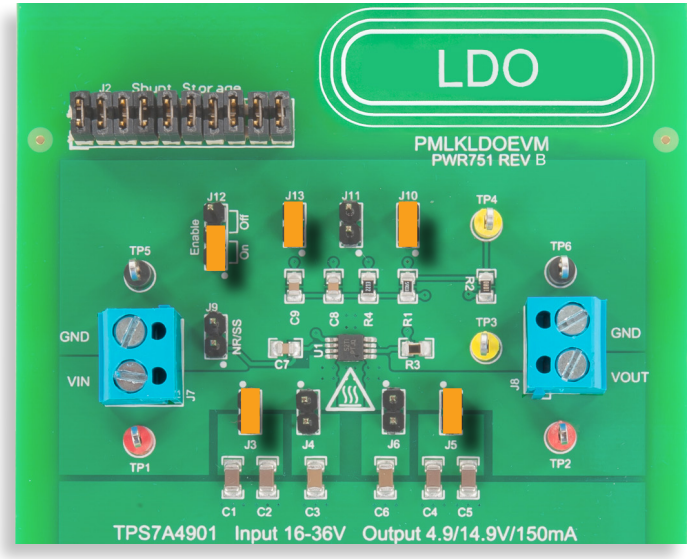


Figure 6. TPS7A4901 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 6):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7μF) and C_5 (4.7μF) output capacitors connected
- J_3 **shorted** → C_1 (4.7μF) and C_2 (4.7μF) input capacitors connected
- J_4 **open** → C_3 (2.2μF) input capacitor disconnected
- J_6 **open** → C_6 (2.2μF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the OSCILLOSCOPE, set CH-1 in DC 50Ω coupling mode, select CH-1 as trigger source, execute the "de-gauss" of the current probe to remove possible dc bias in the current probe, set CH-2 in DC 1MΩ coupling mode, CH-3 in AC 1MΩ coupling mode and CH-4 in DC 1MΩ coupling mode
2) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the DC VOLTAGE at 6V, and set the CURRENT LIMIT at 200mA
3) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the DYNAMIC CURRENT MODE and fix:
   - low current level at 50mA and low current time at 10ms
   - high current level at 150mA and high current time at 10ms
   - current rise and fall slew-rates at the highest level allowed by the instrument
4) turn ON the POWER SUPPLY "OUT ON" button. In these conditions you should see on the OSCILLOSCOPE the traces of CH-1 (load current) and CH-3 (AC component of output voltage) as flat horizontal lines at 0 level, the trace of CH-2 (DC+AC components of the output voltage) as a flat line at 5V level, and the trace of CH-4 (input voltage) as a flat line at 6V level. Use the OSCILLOSCOPE cursors (or measurement functions) to verify the values of the average input and output voltages. If you read value much different than the expected ones, turn OFF the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps
5) turn ON the ELECTRONIC "LOAD ON" button. In these conditions you should see CH-1 trace as a square-wave, CH-2 trace as a flat line with 5V average value, CH-3 trace as a flat line with 0V average value and small magnitude spikes of short duration in correspondence of load current transients, and CH-4 trace as a flat line at 6V level (see the experimental figures samples at the end of the experiment). Expand the vertical scale and adjust the off-set of the four channels and the time-scale to make the waveforms best fitting the scope width and height. Adjust the trigger level at 50% of the CH-1 trace vertical swing
6) record in Table 1 the output voltage average value before and after each load transient and the output voltage transient surge magnitude for the input voltage values listed in Table 1 (you do not need to turn OFF the POWER SUPPLY "OUT ON" button while adjusting the voltage)
7) turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then short jumper J_{11} to connect C_8 (100nF) phase lead capacitor in parallel to C_9 (12nF) phase lead capacitor, repeat the steps 4) to 6), and report the results in Table 2
8) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

1) Measure the DC output voltage $V_{OUTinitial}$ before the load transient, the DC output voltage $V_{OUTfinal}$ the LDO regulator provides at the end of the load transient, the magnitude of the output voltage surge ΔV_{OUT} during the the load transient response, and collect the measurements in Tables 1 and 2.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][12].

Table 1. Load transient performance of TI-PMLK TPS7A4901 LDO regulator at V_{OUT} = 5V, with C_9 (12nF) phase lead capacitor connected

(1) $V_{OUTinitial}$ [V]	(2) $V_{OUTfinal}$ [V]	(3) ΔV_{OUT} surge [mV]	V_{IN} = 6V			V_{IN} = 12V			V_{IN} = 18V		
I_{OUT}: 50mA→150mA			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)
I_{OUT}: 150mA→50mA			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)

Table 2. Load transient performance of TI-PMLK TPS7A4901 LDO regulator at V_{OUT} = 5V, with C_8 (100nF) and C_9 (12nF) phase lead capacitors connected in parallel

(1) $V_{OUTinitial}$ [V]	(2) $V_{OUTfinal}$ [V]	(3) ΔV_{OUT} surge [mV]	V_{IN} = 6V			V_{IN} = 12V			V_{IN} = 18V		
I_{OUT}: 50mA→150mA			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)
I_{OUT}: 150mA→50mA			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)

Output capacitors:

J_5 shorted and J_6 open:
$C_{out} = C_4$ and C_5 in parallel = 9.4µF
ESR ~ 35mΩ@10kHz, ~2mΩ@1MHz

J_5 open and J_6 shorted:
$C_{out} = C_6$ = 2.2µF
ESR ~ 50mΩ@10kHz, ~4mΩ@1MHz

J_5 shorted and J_6 shorted:
$C_{out} = C_4$, C_5 and C_6 in parallel = 11.6µF
ESR ~20mΩ@10kHz, 1.5mΩ@1MHz

Phase lead capacitors:

J_{11} open and J_{13} shorted:
$C_{FF} = C_9$ = 12nF

J_{11} shorted and J_{13} open:
$C_{FF} = C_8$ = 100nF

J_{11} shorted and J_{13} shorted:
$C_{FF} = C_8$ and C_9 in parallel = 112nF

TPS7A4901:
ω_{OA} ~ 0.12-0.15Mrad/s
ω_Z ~ 1.2-1.5Mrad/s [$\omega_Z = 1/(R_{comp}C_{comp})$]
ω_{Ppwr} ~ 12-15Mrad/s

Answer:

1. Does the output voltage exhibit oscillations during load transients? ☐ yes ☐ no ☐ it depends on: _____

2. Does the final output voltage $V_{OUTfinal}$ value equal the initial one $V_{OUTinitial}$? ☐ yes ☐ no ☐ it depends on: _____

3. Describe the correlation of the surge magnitude ΔV_{OUT} with the input voltage, the polarity of the load step and the phase lead capacitor setup: _____

Test#2: preparation and procedure

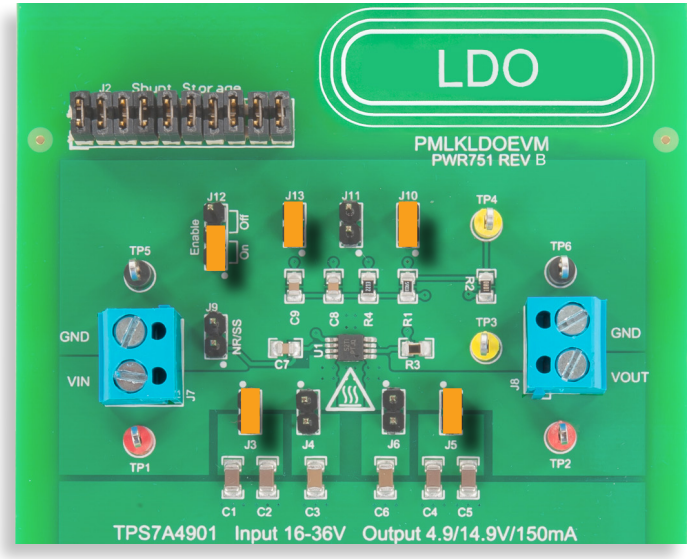


Figure 7. TPS7A4901 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 7):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7μF) and C_5 (4.7μF) output capacitors connected
- J_3 **shorted** → C_1 (4.7μF) and C_2 (4.7μF) input capacitors connected
- J_4 **open** → C_3 (2.2μF) input capacitor disconnected
- J_6 **open** → C_6 (2.2μF) output capacitor disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the OSCILLOSCOPE, set CH-2 in DC 1MΩ coupling mode, set CH-3 in AC 1MΩ coupling mode, set CH-4 in DC 1MΩ coupling mode, and select CH-4 as trigger source
2) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the dynamic MODE and fix:
   - low voltage level at 6V and low voltage time at 10ms
   - high voltage level at 8V and high voltage time at 10ms
   - voltage rise and fall slew-rates at the highest level allowed by the instrument
   - the CURRENT LIMIT at 200mA
3) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the DC CURRENT MODE and set the current level at 1mA
4) turn ON the POWER SUPPLY "OUT ON" button and the ELECTRONIC "LOAD ON" button. In these conditions you should see on the OSCILLOSCOPE the trace of CH-2 (full output voltage) as a flat line at 5V level, the trace of CH-3 (AC component of output voltage) as a flat line with 0V average value and small magnitude spikes of short duration in correspondence offline voltage transients and the trace of CH-4 (input voltage) as a square-wave. Expand the vertical scale and adjust the off-set of the OSCILLOSCOPE channels and the time-scale to make the waveforms fitting the scope width and height. Adjust the trigger level at 50% of the CH-4 trace vertical swing
5) use OSCILLOSCOPE cursors, or measurement functions, to measure the output voltage average value before and after each line transients and the output voltage transient peak surge magnitude for the load current values listed in Table 3 (you do not need to turn OFF the ELECTRONIC LOAD "LOAD ON" button while adjusting the voltage)
6) record in Table 3 the output voltage average value before and after each load transient and the output voltage transient surge magnitude for the input voltage values listed in Table 3 (you do not need to turn OFF the POWER SUPPLY "OUT ON" button while adjusting the voltage)
7) turn OFF the ELECTRONIC LOAD "LOAD ON" button and the DC POWER SUPPLY "OUT ON" button, then short jumper J_6 to connect C_6 (2.2μF) output capacitor, open jumper J_5 to disconnect C_4 (4.7μF) and C_5 (4.7μF) output capacitors and repeat the steps 4) to 7), using Table 4 for results
8) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) Measure the DC output voltage $V_{OUTinitial}$ before the line transient , the DC output voltage $V_{OUTfinal}$ the LDO regulator provides at the end of the line transient, the magnitude of the output voltage surge ΔV_{OUT} during the the line transient response, and collect the measurements in Tables 3 and 4.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [1][2][4].

Table 3. Line transient performance of TI-PMLK TPS7A4901 LDO regulator at V_{OUT} = 5V, with C_4 (4.7µF) and C_5 (4.7µF) output capacitors connected

(1) $V_{OUTinitial}$ [V]	(2) $V_{OUTfinal}$ [V]	(3) ΔV_{OUT} surge [mV]	I_{OUT} = 1mA			I_{OUT} = 50mA			I_{OUT} = 100mA		
V_{IN}: 6V→8V			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)
I_{OUT}: 8V→6V			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)

Table 4. Line transient performance of TI-PMLK TPS7A4901 LDO regulator at V_{OUT} = 5V, with C_6 (2.2µF) output capacitor connected

(1) $V_{OUTinitial}$ [V]	(2) $V_{OUTfinal}$ [V]	(3) ΔV_{OUT} surge [mV]	I_{OUT} = 1mA			I_{OUT} = 50mA			I_{OUT} = 100mA		
V_{IN}: 6V→8V			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)
I_{OUT}: 8V→6V			(1)	(2)	(3)	(1)	(2)	(3)	(1)	(2)	(3)

Output capacitors:

J_5 shorted and J_6 open:
$C_{out} = C_4$ and C_5 in parallel = 9.4µF
ESR ~ 35mΩ@10kHz, ~2mΩ@1MHz

J_5 open and J_6 shorted:
$C_{out} = C_6$ = 2.2µF
ESR ~ 50mΩ@10kHz, ~4mΩ@1MHz

J_5 shorted and J_6 shorted:
$C_{out} = C_4$, C_5 and C_6 in parallel = 11.6µF
ESR ~20mΩ@10kHz, 1.5mΩ@1MHz

Phase lead capacitors:

J_{11} open and J_{13} shorted:
$C_{FF} = C_9$ = 12nF

J_{11} shorted and J_{13} open:
$C_{FF} = C_8$ = 100nF

J_{11} shorted and J_{13} shorted:
$C_{FF} = C_8$ and C_9 in parallel = 112nF

TPS7A4901:
ω_{OA} ~ 0.12-0.15Mrad/s
ω_Z ~ 1.2-1.5Mrad/s [$\omega_Z = 1/(R_{comp}C_{comp})$]
ω_{Ppwr} ~ 12-15Mrad/s

Answer:

1. Does the output voltage exhibit oscillations during line transients? ☐ yes ☐ no ☐ it depends on: _____

2. Does the final output voltage $V_{OUTfinal}$ value equal the initial one $V_{OUTinitial}$? ☐ yes ☐ no ☐ it depends on: _____

3. Describe the correlation of the surge magnitude ΔV_{OUT} with the load current, the polarity of the line step and the output capacitor setup: _____

Discussion

In Test#1 we are interested in investigating correlations among the load transient response of the LDO regulator, the values of the input voltage, the polarity of load step and the value of the phase lead capacitance.

The stability of LDO regulators is discussed in [1][4][12], where it is highlighted that the capacitance and ESR of the output capacitor must be bounded within a given range to achieve stability. The internal compensation setup of the TPS7A4901 LDO regulator is designed to guarantee the stability with a capacitance higher than 2.2µF and an ESR lower than 200mΩ [2]. The external phase lead capacitance C_{FF} may help in improving the transient and ac performance of the TPS7A4901 LDO regulator [2]. Stability is ensured in the operating conditions of Test#1. The correlations among the load transient performance and the test conditions depend on the voltage loop gain cross-over frequency. The load current and the output capacitance and ESR are major contributors to the value of the cross-over frequency. The cross-over frequency of the LDO regulator voltage loop gain can be adjusted by means of the placement of the poles and zeros of the feedback compensation error amplifier shown in Figure 1. Given the output capacitance and ESR, if the poles and zeros of the error amplifier are placed so as to set a high cross-over frequency, the loop gain will have a higher magnitude over a wider frequency range, as the loop gain magnitude is greater than 0dB in the range of frequency $[0,\omega_c]$rad/s (*see [7] for details about the design of the error amplifier*). This involves that the effects of load perturbances are more strongly magnified by the error amplifier, by changing more intensely its output voltage, which drives the base current of the PNP pass device, thus determining a faster adaptation of the pass device current to the load demand. Therefore, a higher crossover frequency ensures a faster response of the LDO regulator to load transients. This makes the magnitude of the output voltage transient surges smaller. In fact, the LDO regulator reacts faster to the load perturbation and this shortens the duration of the time interval wherein the output capacitor has to sustain the unbalance between the pass device current and the load current. Therefore, a little correlation is expected between the load transient response of the LDO regulator and the input voltage V_{IN}, as the input voltage mainly influences the PNP pass device bias point and losses (*Experiment 2*). A major correlation is expected, instead, with the phase lead capacitance, as it influences the frequency of the zero $\omega_{ZFF} = 1/(C_{FF}R_{f1})$ of the voltage feedback loop gain. In fact, a decrease of ω_{ZFF} frequency involves a higher voltage feedback loop gain cross-over frequency and then a faster response, with consequent decrease of the load transient output voltage surge magnitude, as shown in Figures 8 and 9. Based on the formula provided in the *Theory Background* section, a higher current increases the frequency of the pole $\omega_{Pload} = I_{OUT}/(C_{OUT}V_{OUT})$, thus determining an increase of the cross-over frequency ω_c and a smaller output voltage surge magnitude. Thus, the load transient might be characterized by a smaller surge when the load current steps down compared to a load current step up, as shown in Figure 8. In principle, given the DC gain T_o, the poles $\{\omega_{Pload}, \omega_{Ppwr}, \omega_{OA}\}$ and the zeros $\{\omega_Z, \omega_{Zff}\}$ of the voltage loop gain formula (1) provided in the *Theory Background* section, the cross-over frequency ω_c could be calculated by solving the equation $|T(\omega_c)|=1$. However, an explicit solution of this equation is not available. If the aforementioned loop gain parameters are available, the cross-over frequency can be determined by means of tranfer functions Bode Plots MATLAB® capabilities [6], looking at the magnitude 0dB crossing point. If the parameters are not available, the loop gain can be measured by means of a network vector analyzer using the 10Ω injection resistor R_2 [8].

In Test#2 we are interested in investigating correlations between the line transient response of the LDO regulator and the values of the load current and of the output capacitance.

The correlation of line transient response with the load current is the same discussed above for the load transient. The line transient response is influenced by the output capacitance, as it influences the $\omega_{Pload} = I_{OUT}/(C_{OUT}V_{OUT})$ pole frequency of the voltage feedback loop gain. A higher output capacitance involves a decrease of ω_{Pload} frequency, and then a lower loop gain cross-over frequency, which causes an increase of the output voltage line transient surges magnitude. Instead, line voltage step-up and line voltage step-down should not determine different output voltage surge magnitudes, as the input voltage mainly influences the PNP pass device bias point and losses (*Experiment 2*). It should be noted that the LDO regulator has a very good line-transient response, so that line transient voltage surges are not visible and measurable if a dynamic source with low voltage slew rate (<1V/µs) is used, as shown in Figures 10 and 11. In most applications of practical interest, sharp step-wise line transients do not occurr, as the slew rate of the output voltage of voltage sources is limited by their output capacitance. So, it is possible that in this test you observe no change in the line transient response after you change the output capacitance setup. However, the sensitivity of the output voltage to high frequency line disturances is one of the most important LDO regulator issues, as LDOs are often used as post-regulators for switching power supplies, to reduce the effects of high switching frequency noise. The LDO regulator line noise rejection capabilities and the relevant impact of the output capacitance are discussed in *Experiment 4* (*see TI-PMLK BUCK, BOOST and BUCK-BOOST to gain insight the switching power supplies issues*).

Experimental plots

The plots collected in the Figures 8 to 11 show some examples of load and line transient response of the TPS7A4901 LDO regulator (*see [2] for further details*).

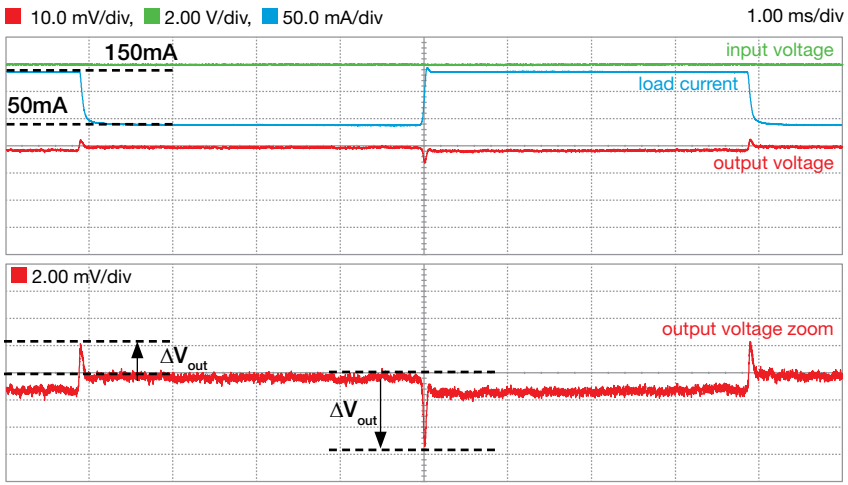


Figure 8. TPS7A4901 LDO load transient for: V_{out}=5V, V_{in}=6V, C_{out}=9.4µF, C_{FF}=100nF and I_{OUT} swinging between 50mA and 150mA

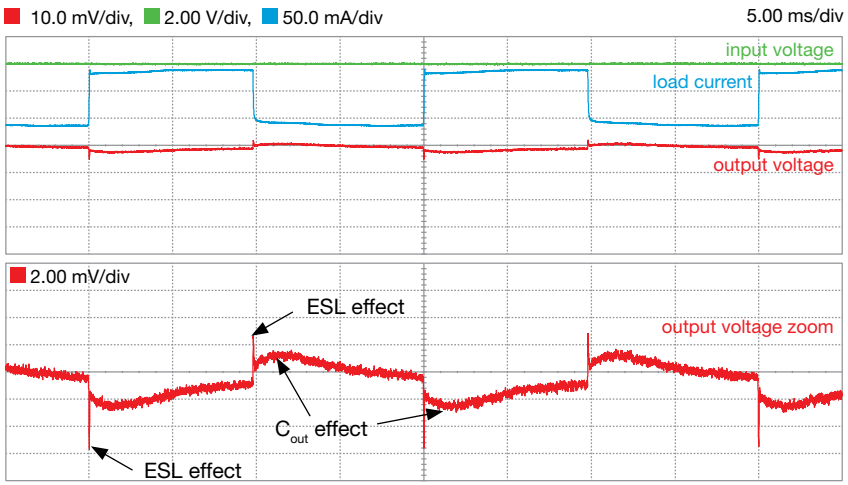


Figure 9. TPS7A4901 LDO load transient for: V_{out}=5V, V_{in}=6V, C_{out}=11.6µF, C_{FF}=12nF and I_{OUT} swinging between 50mA and 150mA

The plots of Figures 8 and 9 highlight the influence of the phase lead capacitance on the TPS7A4901 LDO regulator load tansient response. The output voltage surge magnitude is smaller when the phase lead capacitance is higher, as the frequency of the zero ω_{ZFF} is lower, thus increasing the cross-over frequency. It can be noticed that the overshoot and undershoot surge magnitudes are referred to the zero level of the AC component of the output voltage. Indeed, the load transient response of the TPS7A4901 LDO regulator shown in Figures 8 and 9 have been realized by means of a 125Hz and 50Hz square-wave dynamic load current, respectively, in order to easily visualize the step-up and the step-down load transients in the same oscilloscope screenshot. Therefore, each load step occurs before the transient response to the previous load step has completely vanished. A square-wave dynamic load current with a frequency lower than 5Hz allows the observation of the complete transient response. In Figure 9 the distinct effects of ESL and C_{out} on the output voltage overshoots and undershoots are highlighted.

Experimental plots

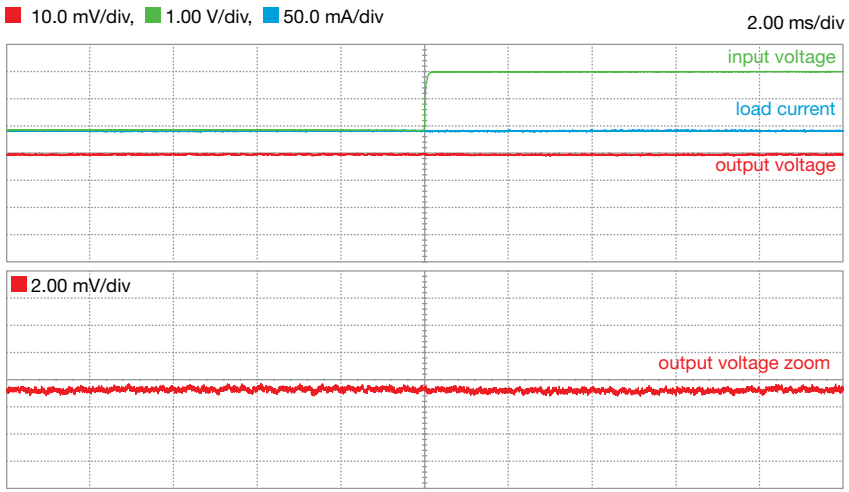


Figure 10. TPS7A4901 LDO line transient for V_{out}=5V, I_{OUT}=50mA, C_{FF}=12nF and V_{IN} rising from 6V to 8V

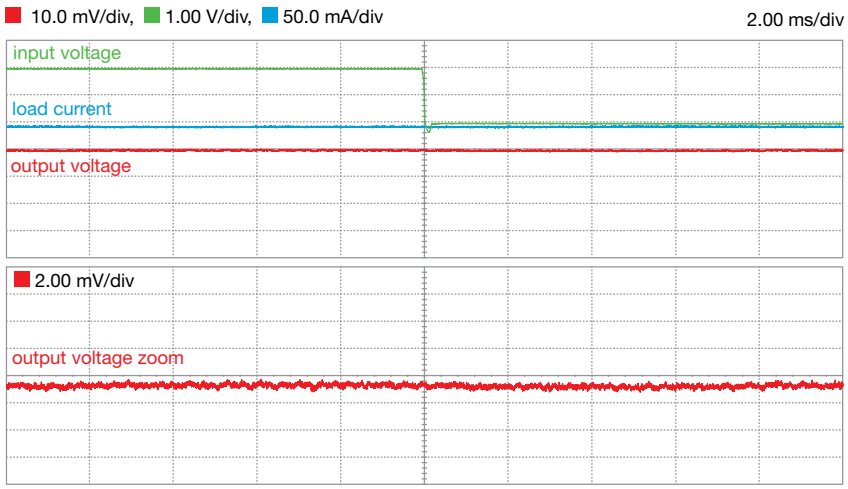


Figure 11. TPS7A4901 LDO line transient for V_{out}=5V, I_{OUT}=50mA, C_{FF}=12nF and V_{IN} falling from 8V to 6V

The plots of Figures 10 and 11 show the line transient response of the TPS7A4901 LDO regulator. No output voltage surges are visible due to the low slew-rate of the input voltage step-up and step-down perturbations (~0.01V/µs).

Experiment 4

The goal of this experiment is to analyze the LDO regulator Power Supply Rejection Ratio (PSRR), that provides a measure of the input noise rejection capabilities of the LDO regulator. The influence of output capacitor and voltage loop phase lead capacitor on the PSRR is investigated. The TPS7A4901 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze the LDO regulator output voltage waveform when an AC noise is injected into the input voltage.

The subject of investigation in this experiment is the line voltage noise rejection capability of the LDO regulator. The LDO regulator is able to guarantee a good output voltage regulation under steady-state (*see Experiment 1 and Experiment 2*) as in presence of line voltage and load current perturbations (*see Experiment 3*). In many applications there are perturbations that are characterized by a moderate magnitude and some dominant harmonic spectrum. This is the case of switching and resonant power supplies, whose DC output voltage exhibits an inherent ripple with a fundamental frequency that can range from 10kHz to about 10MHz. LDO regulators are ideal as post-regulators to filter out high frequency ripple noise in powering analog-to-digital converters and other noise-sensitive devices in audio, measurement and RF applications, where high accuracy is needed.

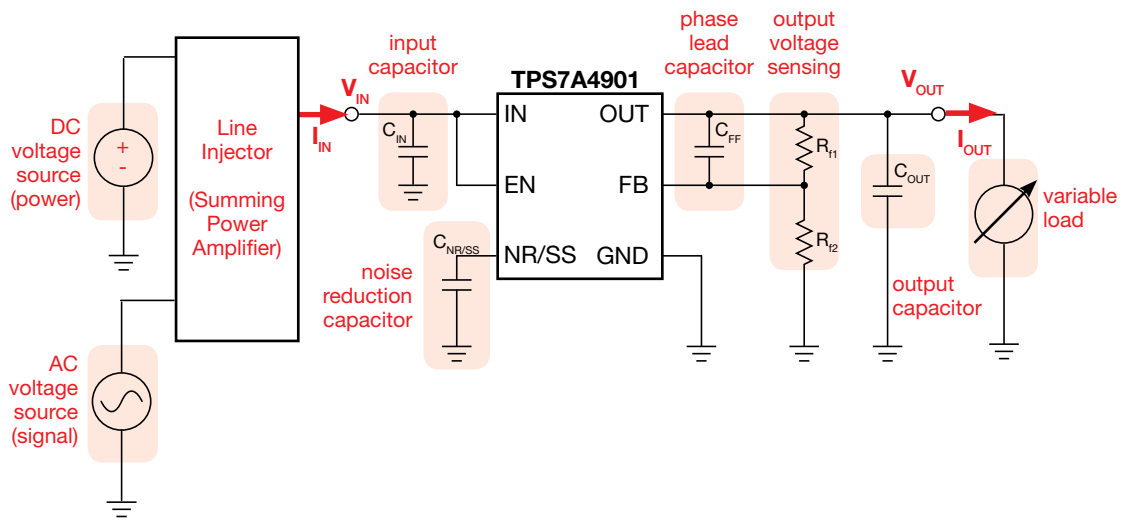


Figure 1. Simplified schematic of the TPS7A4901 LDO regulator

Test#1. We set up the TPS7A4901 LDO regulator with an input voltage consisting of an AC component added to a DC voltage and terminate it into a fixed DC load, as shown in Figure 1. The input voltage AC component is added by means of a Line Injector, which is a device able to apply an AC noise on the DC voltage generated by the DC voltage source. The LDO regulator is terminated into an adjustable load. We record the PSRR over a wide frequency range, varying the DC bias voltage values and different values of output capacitance C_{OUT}. The influence of the DC voltage and of the output capacitance C_{OUT} on the PSRR magnitude will be observed and discussed.

Test#2. We set up the TPS7A4901 LDO regulator with an input voltage consisting of an AC component added to a fixed DC bias voltage and terminate it into an adjustable DC load. Then we record the PSRR over a wide frequency range, varying the load current and the value of the phase lead capacitance CFF. The influence of the load current and of the phase lead capacitance CFF on the PSRR magnitude will be observed and discussed.

Theory Background

The fundamentals of LDO regulators Power Supply Rejection Ratio are provided in this section *(see [1][4][11][12] for a general discussion of LDO regulators operation and characteristics, [5] for a discussion on PSRR measurement, and [2] for more details on TPS7A4901 operation and features).*

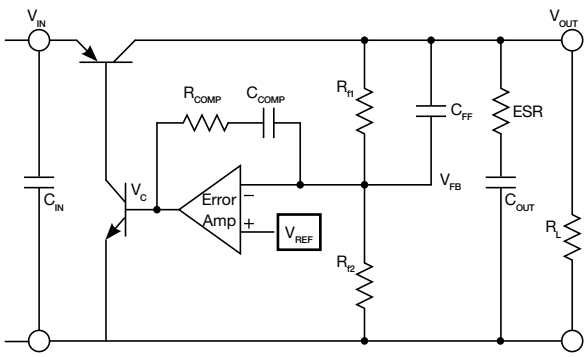


Figure 1

Figure 1 shows the feedback of an LDO regulator with PNP bipolar transistor pass device. The input noise rejection of an LDO regulator is determined by the output capacitor (C_{OUT}, ESR) the feedback loop setup (R_{COMP}, C_{COMP}, R_{f1}, C_{FF}) and by the input capacitor C_{IN}. A high loop-gain cross-over frequency and a big input capacitance C_{IN} improve the noise rejection. However, a too high cross-over may compromise the stability and a too big C_{IN} may cause unwanted resonance with parasitic inductance of input traces and wires. **The PSRR has to be measured with the input capacitor C_{IN} disconnected to assess the inherent LDO input noise rejection capability.**

The efficacy of the LDO regulator in rejecting the input noise is measured through the Power Supply Rejection Ratio (PSRR), which is defined as:

$$PSRR_{dB} = 20\log\left[\frac{\Delta V_{IN,pk-pk}}{\Delta V_{OUT,\,pk-pk}}\right] \quad (1)$$

Figure 2 shows a simple setup to add AC noise to the bias DC input voltage of an LDO regulator. It allows the use of an oscilloscope to probe V_{IN} and V_{OUT} and works within a frequency range that is conditioned by the values of L and C. Though very simple, the PSRR measurement based on L-C elements is affected by bandwidth limits and poor accuracy at low and high frequencies. The use of an input summing power amplifier or line injector provides more reliable measurements over a wider frequency range.

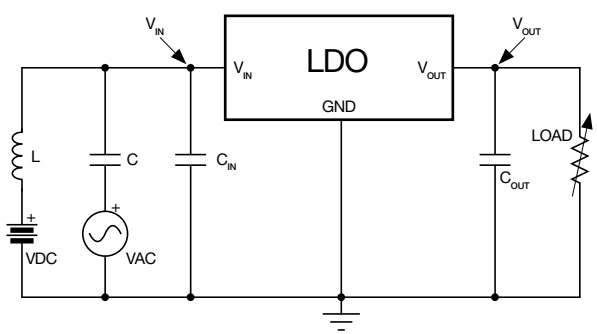


Figure 2

Figure 3 shows the PSRR Bode plots for two different values of output capacitance C_{OUT} and phase-lead capacitance C_{FF}. Increasing the output capacitance C_{OUT} causes a reduction of the cross-over frequency, due to the lower value of the load pole frequency $\omega_{Pload}=I_{out}/(C_{OUT}V_{out})$, and may worsen the PSRR at middle and very high frequencies, whereas the PSRR beyond the cross-over frequency is improved. Increasing the phase lead capacitance C_{FF} determines an increase of the cross-over frequency, due to the lower value of the phase lead zero frequency $\omega_{Pload}=1/(C_{FF}R_{f1})$, and then a better PSRR at low frequencies, whereas high frequency PSRR is not improved.

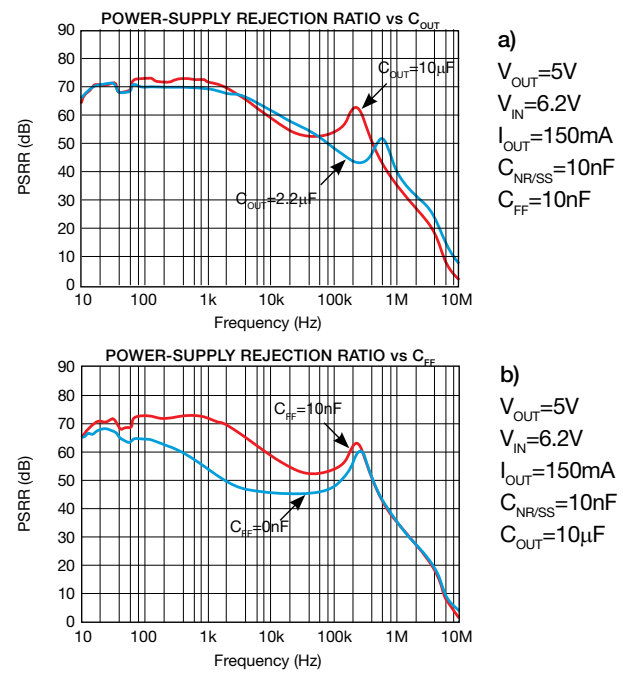


Figure 3

Experiment set-up: configuration

The instruments needed for this experiment are: a DC POWER SUPPLY, a DC ELECTRONIC LOAD, a NETWORK VECTOR ANALYZER, and a LINE INJECTOR. Figure 5 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

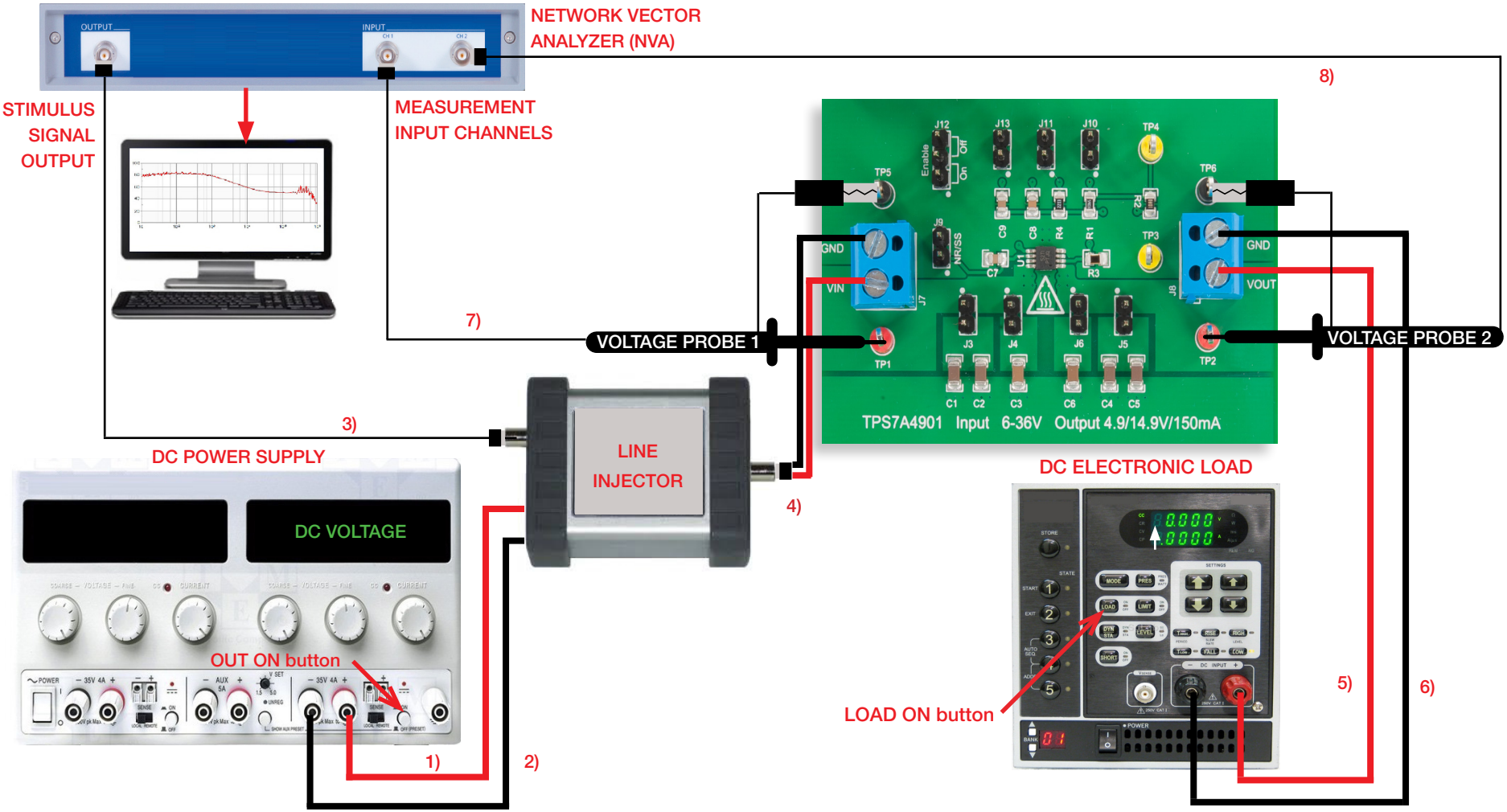


Figure 5. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the positive (RED) output of the DC POWER SUPPLY to the POSITIVE (RED) INPUT of the LINE INJECTOR

2) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the NEGATIVE (BLACK) INPUT of the LINE INJECTOR

3) connect the STIMULUS SIGNAL OUTPUT of the NETWORK VECTOR ANALYZER to the SIGNAL INPUT of the LINE INJECTOR

4) connect the positive output of the LINE INJECTOR to the INPUT (VIN) of the J_7 screw terminal of the TPS7A4901 LDO regulator and the negative output of the LINE INJECTOR to the GROUND (GND) of the J_7 screw terminal of the TPS7A4901 LDO regulator

5) connect the OUTPUT (VOUT) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD

6) connect the GROUND (GND) of the J_8 screw terminal of the TPS7A4901 LDO regulator to the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD

7) connect a voltage probe to channel 1 of the NETWORK VECTOR ANALYZER and hang it to TEST PIN TP_1 which is the input voltage of the TPS7A4901 LDO regulator [WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

8) connect a voltage probe to channel 2 of the NETWORK VECTOR ANALYZER and hang it to TEST PIN TP_2 which is the output voltage of the TPS7A4901 LDO regulator [WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

NOTES:

- Depending on the type of NETWORK VECTOR ANALYZER, you may have a scope embedded in the instrument where you will see the measured PSRR, or you may have a USB (or other type) connection to a personal computer with dedicated interface software for the instrument set-up and PSRR visualization.
- The output impedance of the LINE INJECTOR can be slightly resistive.
- The input capacitor on the LDO regulator, working as a low pass filter, influences the PSRR. Therefore, the PSRR measurements may change depending on whether they are performed with or without the input capacitor connected.

Test#1: preparation and procedure

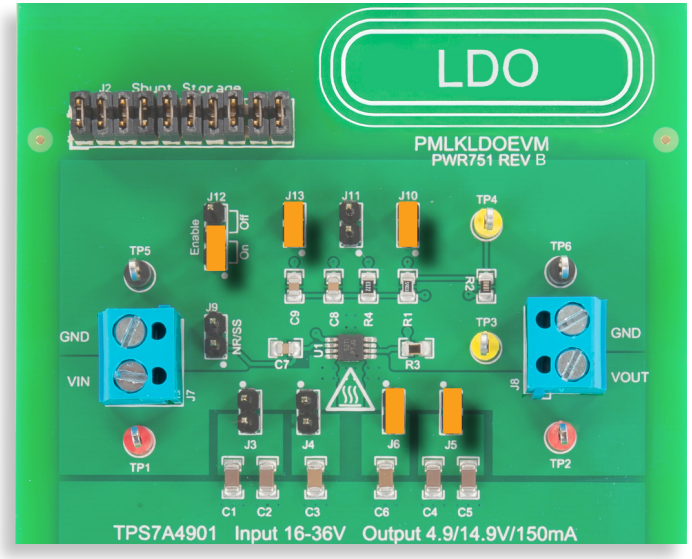


Figure 6. TPS7A4901 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 6):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7µF) and C_5 (4.7µF) output capacitors connected
- J_6 **shorted** → C_6 (2.2µF) output capacitor connected
- J_4 **open** → C_3 (2.2µF) input capacitor disconnected
- J_3 **open** → C_1 (4.7µF) and C_2 (4.7µF) input capacitors disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the NETWORK VECTOR ANALYZER
2) set the measurement frequency range from 10Hz to 10MHz
3) follow the NETWORK VECTOR ANALYZER user's manual instructions to set the magnitude of the output AC signal and the gain of the output and input channels. [NOTE: a high magnitude of the output AC signal improves the efficacy of the PSRR measurement. Nevertheless, the swing of the AC signal has to be limited to guarantee that the LDO regulator input voltage does not drop below the dropout voltage, when the DC component is low]
4) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the voltage at 8V and set the CURRENT LIMIT at 200mA
5) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the DC current MODE and set the current level at 25mA
6) turn ON the POWER SUPPLY "OUT ON" button and turn ON the ELECTRONIC LOAD "LOAD ON" button
7) in these conditions you should see on the NETWORK VECTOR ANALYZER screen/interface a crispy horizontal line: the instrument is measuring just noise
8) turn ON the NETWORK VECTOR ANALYZER "SWEEP ON" button
9) in these conditions you should see on the NETWORK VECTOR ANALYZER screen/interface a PSRR MAGNITUDE plot similar to the red line plotted in Figure 3 (if the plot looks completely different, turn OFF the "SWEEP ON" button of the NETWORK VECTOR ANALYZER, the "LOAD ON" button of the DC ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps)
10) use the NETWORK VECTOR ANALYZER cursors to measure the PSRR values at the values of frequency listed in Table 1
11) repeat step 10) for the DC input voltage listed in Table 1 (you do not need to turn OFF the POWER SUPPLY "OUT ON" button while adjusting the voltage of the DC POWER SUPPLY)
12) turn OFF the "SWEEP ON" button of the NETWORK VECTOR ANALYZER, the "LOAD ON" button of the DC ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, open jumper J_5 to disconnect C_4 (4.7µF) and C_5 (4.7µF) output capacitors and repeat the steps 6) to 11)
13) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

1) Measure the PSRR at the frequencies listed in the Table 1, with the two different output capacitor setups.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [2][9][12].

Table 1. PSRR of the TPS7A4901 LDO regulator with V_{OUT} = 5V, I_{out} = 25mA, C_{FF} = 12nF and different output capacitors setup

(1) PSRR [dB] with C_{OUT}=2x4.7µF+2.2µF	AC signal frequency				
(2) PSRR [dB] with C_{OUT}=2.2µF	100Hz	1kHz	10kHz	100kHz	1MHz
$V_{IN,DC}$ = 8V	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)
$V_{IN,DC}$ = 12V	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)
$V_{IN,DC}$ = 16V	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)

Output capacitors:

J_5 shorted and J_6 open:
C_{out} = C_4 and C_5 in parallel = 9.4µF
ESR ~ 35mΩ@10kHz, ~2mΩ@1MHz

J_5 open and J_6 shorted:
C_{out} = C_6 = 2.2µF
ESR ~ 50mΩ@10kHz, ~4mΩ@1MHz

J_5 shorted and J_6 shorted:
C_{out} = C_4, C_5 and C_6 in parallel = 11.6µF
ESR ~20mΩ@10kHz, ~1.5mΩ@1MHz

Phase lead capacitors:

J_{11} open and J_{13} shorted:
C_{FF} = C_9 = 12nF

J_{11} shorted and J_{13} open:
C_{FF} = C_8 = 100nF

J_{11} shorted and J_{13} shorted:
C_{FF} = C_8 and C_9 in parallel = 112nF

(Visit the websites of capacitors manufacturers for more details about ESR vs frequency curves)

Answer:

1. How does the PSRR Magnitude depend on the output capacitance? ☐ insensitive ☐ increases with higher capacitance ☐ decreases with higher capacitance

   ☐ other: _____

2. Is the DC input voltage $V_{IN,DC}$ influential on output voltage surge magnitude? ☐ yes ☐ no ☐ it depends on load current ☐ other:

   _____

Test#2: preparation and procedure

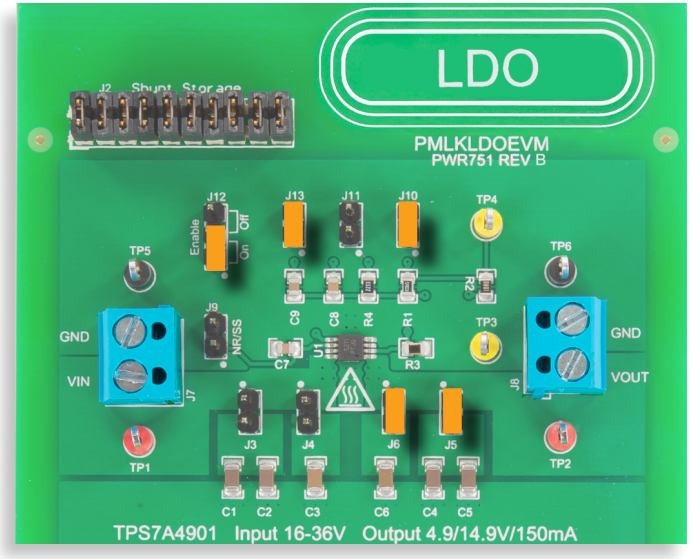


Figure 7. TPS7A4901 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 7):

- J_{12} **shorted** in **ON** position → LDO operation enabled
- J_{10} **shorted** → nominal output voltage V_{out} = 5V
- J_{13} **shorted** → C_9 (12nF) phase lead capacitor connected
- J_5 **shorted** → C_4 (4.7µF) and C_5 (4.7µF) output capacitors connected
- J_6 **shorted** → C_6 (2.2µF) output capacitor connected
- J_4 **open** → C_3 (2.2µF) input capacitor disconnected
- J_3 **open** → C_1 (4.7µF) and C_2 (4.7µF) input capacitors disconnected
- J_{11} **open** → C_8 (100nF) phase lead capacitor disconnected
- J_9 **open** → C_7 (12nF) noise reduction capacitor disconnected

Test Procedure:

1) turn on the NETWORK VECTOR ANALYZER
2) set the measurement frequency range from 10Hz to 10MHz
3) follow the NETWORK VECTOR ANALYZER user's manual instructions to set the magnitude of the output AC signal and the gain of the output and input channels. [NOTE: a high magnitude of the output AC signal improves the efficacy of the PSRR measurement. Nevertheless, the swing of the AC signal has to be limited to guarantee that the LDO regulator input voltage does not drop below the dropout voltage, when the DC component is low]
4) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the voltage at 8V and set the CURRENT LIMIT at 200mA
5) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the DC current MODE and set the current level at 25mA
6) turn ON the POWER SUPPLY "OUT ON" button and turn ON the ELECTRONIC LOAD "LOAD ON" button
7) in these conditions you should see on the NETWORK VECTOR ANALYZER screen/interface a crispy horizontal line: the instrument is measuring just noise
8) turn ON the NETWORK VECTOR ANALYZER "SWEEP ON" button
9) in these conditions you should see on the NETWORK VECTOR ANALYZER screen/interface a PSRR MAGNITUDE plot similar to the red line plotted in Figure 3 (if the plot looks completely different, turn OFF the "SWEEP ON" button of the NETWORK VECTOR ANALYZER, the "LOAD ON" button of the DC ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps)
10) use the NETWORK VECTOR ANALYZER cursors to measure the PSRR values at the values of frequency listed in Table 1
11) repeat step 10) for the DC input voltage listed in Table 1 (you do not need to turn OFF the POWER SUPPLY "OUT ON" button while adjusting the voltage of the DC POWER SUPPLY)
12) turn OFF the "SWEEP ON" button of the NETWORK VECTOR ANALYZER, the "LOAD ON" button of the DC ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, short jumper J_{11} to connect C_8 (100nF) and open jumper J_{13} to disconnect C_9 (12nF) phase lead capacitors and repeat the steps 6) to 11)
13) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) Measure the PSRR at the frequencies listed in the Table 2, with the two different phase lead capacitor setups.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in [2][9][12].

Table 2. PSRR of the TPS7A4901 LDO regulator with V_{OUT} = 5V, I_{out} = 25mA, C_{OUT} = 2x4.7µF+2.2µF and different phase lead capacitors setup

(1) PSRR [dB] with C_{FF} = 12nF	AC signal frequency				
(2) PSRR [dB] with C_{FF} = 100nF	100Hz	1kHz	10kHz	100kHz	1MHz
I_{OUT} = 25mA	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)
I_{OUT} = 75mA	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)
I_{OUT} = 125mA	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)

Output capacitors:

J_5 shorted and J_6 open:
C_{out} = C_4 and C_5 in parallel = 9.4µF
ESR ~ 35mΩ@10kHz, ~2mΩ@1MHz

J_5 open and J_6 shorted:
C_{out} = C_6 = 2.2µF
ESR ~ 50mΩ@10kHz, ~4mΩ@1MHz

J_5 shorted and J_6 shorted:
C_{out} = C_4, C_5 and C_6 in parallel = 11.6µF
ESR ~20mΩ@10kHz, ~1.5mΩ@1MHz

Phase lead capacitors:

J_{11} open and J_{13} shorted:
C_{FF} = C_9 = 12nF

J_{11} shorted and J_{13} open:
C_{FF} = C_8 = 100nF

J_{11} shorted and J_{13} shorted:
C_{FF} = C_8 and C_9 in parallel = 112nF

(Visit the websites of capacitors manufacturers for more details about ESR vs frequency curves)

Answer:

1 Describe the observed correlations among the C_{FF} capacitance, the load current I_{OUT} and the **PSRR** values over the frequency range of measurement:

Discussion

In Test#1 we are interested in investigating correlations between the PSRR of the LDO regulator and the values of the DC input voltage and of the output capacitance.

The PSRR is a measure of the capability of a power supply to ensure the immunity of the output voltage against *permanent disturbances* (ripple noise) in the input voltage, whereas the magnitude of the output voltage surges exhibited during the line transient response, investigated in *Experiment 3*, is a measure of the capability of a power supply to achieve the immunity of the output voltage against *occasional transient disturbances* (spike noise) in the input voltage. The former is based on frequency-domain analysis, the latter is based on time domain analysis. The frequency-domain response and the time-domain response of a dynamic system, like an LDO voltage regulator, are correlated to each other. The factors impacting the LDO regulator time-domain response also do impact its frequency-domain response. In *Experiment 3* it has been highlighted that a higher output capacitance reduces the cross-over frequency of the voltage feedback loop gain, and this is expected to slow down the line transient response, with consequent increase of output voltage surges magnitude. It has been also emphasized that if the cross-over frequency is very high, like for the TPS7A4901 LDO regulator, the line transient output voltage surges may not be visible unless a dynamic source with very high voltage slew rate (>1V/μs) is used. A high slew-rate line voltage disturbance is a form of high frequency noise (the frequency spectrum of a sharp edge step-up waveform has more harmonics than a smooth edge step-up waveform). Thus, if we want to measure the ability of a voltage regulator to immunize its output voltage against fast line transients, we can analyze its PSRR, rather than through a more difficult line transient test. The *closed-loop* PSRR of an LDO regulator plot can be divided in four regions, as shown in Figures 8 and 9. In the DC-to-middle frequency region (a) the *closed-loop* PSRR looks almost flat and its magnitude is determined by the open loop DC gain of the error amplifier. In the middle-to-high frequency region (b) the *closed-loop* PSRR is influenced by the poles and zeros of the feedback loop gain and of the *open-loop* PSRR, which is the PSRR without feedback control. The output capacitor plays a double role in the region (b):

1) it influences the loop gain cross-over frequency and the high-frequency boundary of the middle-to-high frequency region, which corresponds to the cross-over frequency (it is also called “system bandwidth” as it bounds the frequency region where the closed-loop feedback control is able to attenuate the effects of disturbances);
2) it influences the *open-loop* PSRR and the magnitude of the *closed-loop* PSRR nearby the high frequency boundary of the middle-to-high frequency region.

In particular, an output capacitance increase has a beneficial effect on the *open-loop* PSRR at high frequency, where the output capacitor has a lower impedance, whereas it causes a decrease of the closed-loop pole frequency $\omega_{Pload}=I_{OUT}/(C_{OUT}V_{OUT})$, with a consequent reduction of the system bandwidth (see Figures 8 and 9). In the regions (c) and (d) beyond the cross-over frequency the feedback control is inactive and the *closed-loop* PSRR equals the open-loop PSRR. The PSRR rise in the region (c) is determined by the progressive decrease of the output capacitor impedance, whereas the PSRR fall in the region (d) is caused by the capacitances of the pass device and other parasitic.
The input voltage has a minor influence on the PSRR as it mainly determines the bias point of the PNP pass device.

In Test#2 we are interested in investigating correlations between the PSRR of the LDO regulator and the values of the load current and of the phase lead capacitance.

A correlation is expected with the load current, as it influences the ω_{Pload} pole of the voltage loop gain. A higher current involves a higher pole frequency and then a higher cross-over frequency, then a higher PSRR magnitude and an expansion of the system bandwidth.
The phase lead capacitance has a direct impact on the feedback loop gain too, as it determines the position of the zero $\omega_{ZFF}=1/(C_{FF}R_{f1})$. An increase of the phase lead capacitance involves a lower frequency of the zero ω_{ZFF} thus determining a higher loop-gain and a higher PSRR magnitude in the middle-to-high frequency region.

Experimental plots

The plots collected on this page are samples of experimental measurements performed on the TPS7A4901 LDO regulator. They show the PSRR magnitude of the LDO regulator with different line, load and phase lead capacitor setup (*see [4] for further details*).

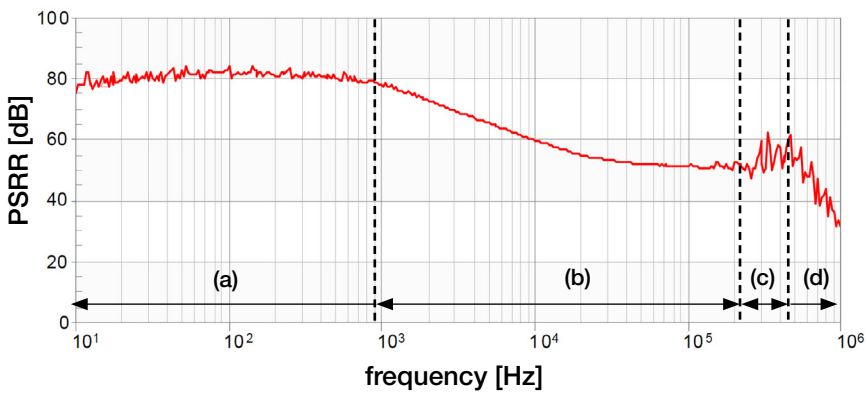


Figure 8. TPS7A4901 LDO PSRR for:
V_{out}=5V, V_{in}=6.5V, I_{out}=100mA, no C_{in}, C_{out}=2x4.7µF, C_{FF}=100nF

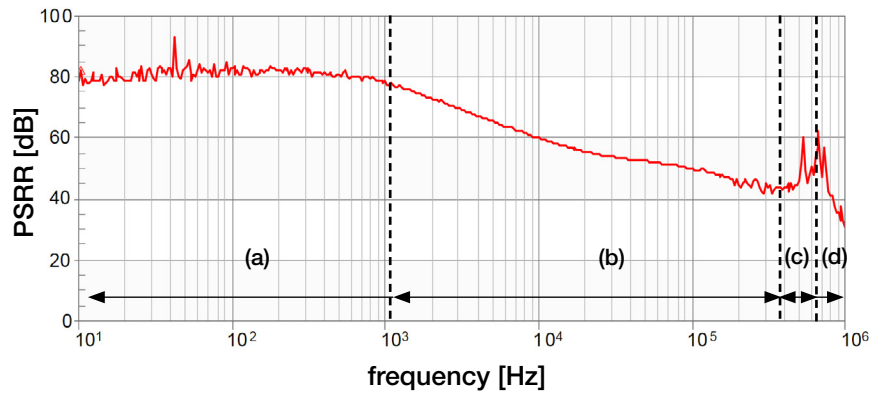


Figure 9. TPS7A4901 LDO PSRR for:
V_{out}=5V, V_{in}=6.5V, I_{out}=100mA, no C_{in}, C_{out}=2.2µF, C_{FF}=100nF

The plots of Figures 8 and 9 highlight the influence of the output capacitance on the TPS7A4901 LDO regulator closed-loop PSRR. In Figure 8 you can observe a lower crossover-frequency (upper boundary of region (b)) and a higher magnitude of the PSRR as in the high frequency range of region (b) as in the region (c), compared to the PSRR plot of Figure 9. These are the effects of the higher capacitance.

NOTE. The PSRR plots look crisp in the low frequency and in the high frequency ranges due to the effects of the measurement system configuration and setup. The plots of Figures 8 to 11 have been realized by means of a network vector analyzer and of a power summing amplifier which adds the ac stimulus generated by the network vector analyzer to the constant voltage generated by the DC power supply, as shown in Figure 1. The ac stimulus frequency sweeps from a lower boundary f_{min} to a higher boundary f_{max}, through a given number N_{sam} of sample frequencies. The magnitude of the ac stimulus can be set at different levels for each sample frequency over the [f_{min},f_{max}] range. For each sample frequency, the network vector analyzer injects the sinusoidal ac stimulus into the line and measures the magnitude of the corresponding sinusoidal disturbance on the output voltage. The sweep time T_{swp} is the time the network vector analyzer takes to execute the PSRR measurement over the entire frequency range [f_{min},f_{max}]. Changing the [f_{min},f_{max}], N_{sam}, T_{swp} and ac stimulus magnitude setup determines different levels of accuracy and smoothness in the PSRR plot. The bandwidth of the power summing amplifier may also influence the high frequency region of the PSRR plot. Finally, output noise-floor level has to be assessed to discern PSRR from the inherent noise of the LDO regulator in the measurement environment. The reader is invited to further investigate LDO regulators PSRR measurements issues in the relevant technical literature [2][9][12].

Experimental plots

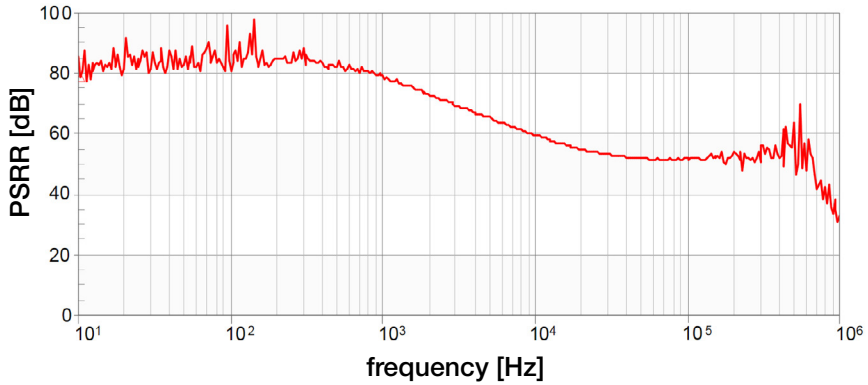


Figure 10. TPS7A4901 LDO PSRR for:
V_{out}=5V, V_{in}=12V, I_{out}=20mA, no C_{in}, C_{out}=2x4.7µF, C_{FF}=100nF

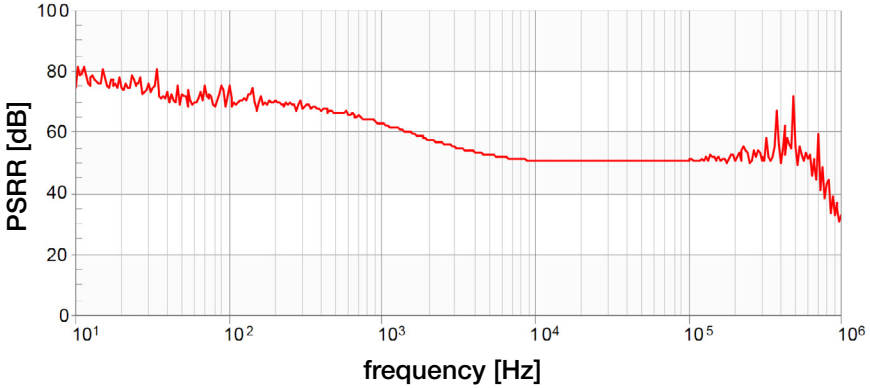


Figure 11. TPS7A4901 LDO PSRR for:
V_{out}=5V, V_{in}=12V, I_{out}=20mA, no C_{in}, C_{out}=2x4.7µF, no C_{FF}

The plots of Figures 10 and 11 highlight the influence of the phase lead capacitance on the TPS7A4901 LDO regulator closed-loop PSRR. In Figure 10 you can observe a higher PSRR, compared to the plot of Figure 11, in the middle-to-high frequency region, where the zero introduced by the phase lead capacitance has a strong effect on the increase of the cross-over frequency, thus improving the PSRR.

Experiment 5

The goal of this experiment is to analyze the dropout voltage and the ground current of an LDO regulator based on a N-channel MOSFET pass device. The TPS7A8300 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze how the dropout voltage and the output voltage accuracy of the N-channel LDO regulator depends on the line and load conditions.

The subject of investigation in this experiment is the measurement of the voltage drop across the N-channel MOSFET pass device when it works in the ohmic region. The pass device voltage drop influences the dropout voltage of the LDO regulator, namely the minimum input voltage allowing the output voltage to be regulated at the desired nominal value. In this experiment the dropout voltage $V_{dropout}$ across the pass device is measured in a different way compared to *Experiment 1*. In particular, as shown in Figure 1, the feedback pin voltage is forced at a value imposed by an external DC signal generator. If we set such value slightly lower than the 0.8V reference voltage, we emulate the effect of having an output voltage lower than the nominal one, thus causing the internal error amplifier to force the pass device to work into the ohmic region, thus allowing the measurement of the dropout voltage associated to the N-channel MOSFET.

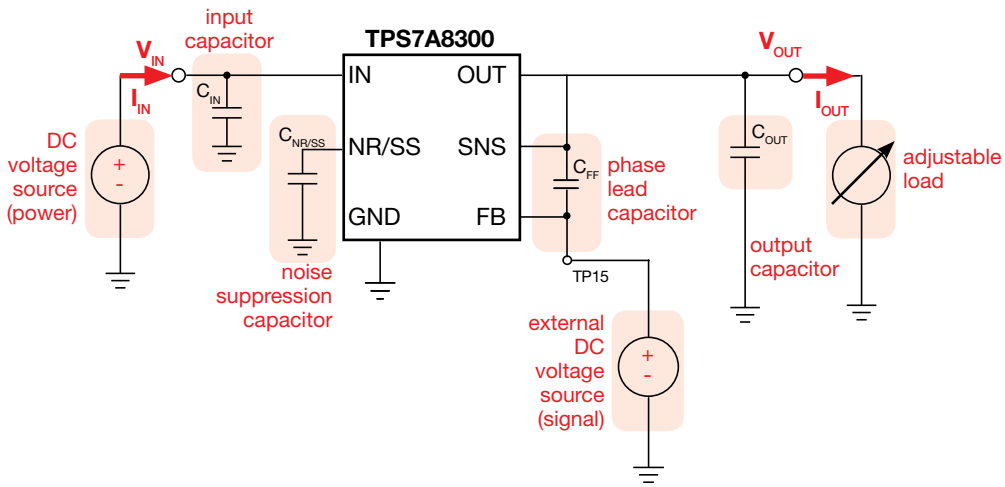


Figure 1. Simplified schematic of the TPS7A8300 LDO regulator

Test#1. We measure the input voltage and the output voltage of the TPS7A8300 LDO regulator at different input voltage and load current, in two different conditions of floating feedback pin and forced feedback pin. The goal is to detect the voltage drop of the N-channel MOSFET pass device of the LDO regulator, to calculate its channel resistance and to observe how it depends on the operating conditions.

Test#2. We measure the ground current of the TPS7A8300 LDO regulator at different input voltage and load current to observe how it depends on the operating conditions.

Theory Background

The fundamentals of N-MOSFET LDO regulators are provided in this section *(see [1][4][11][12] for a general discussion of LDO regulators operation, and [3] for more details on TPS7A8300 operation and features, and refer to Experiment 1 for dropout voltage discussion regarding a PNP pass device LDO regulator).*

Figure 2 shows the internal architecture of the TPS7A8300 LDO regulator, using an N-channel MOSFET pass device.

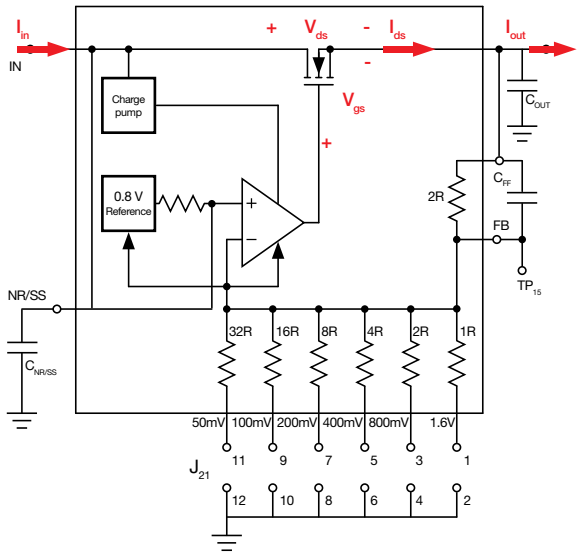


Figure 2

The output voltage can be set from 0.8V to 3.95V with steps of 50mV, by selecting the proper combination of internal resistances 1R to 32R to connect to ground through the jumpers rack J_{24}. In normal operation, the feedback pin FB is floating and the feedback control of Figure 2 senses the output voltage and adjusts the MOSFET gate-source voltage V_{gs} until the drain-source voltage V_{ds} equals the difference between the input voltage and the desired output voltage V_{out}, and the MOSFET drain-source current I_{ds} equals the load current I_{out}, according to equations (1)(2):

(1) $$V_{ds} = V_{drop} = V_{in} - V_{out} = V_{in} - R_{out} I_{out} = V_{in} - R_{out} I_{ds}$$

(2) $$I_{ds} = (V_{in} - V_{ds}) / R_{out}$$

The output voltage is regulated if the MOSFET operates in the saturation region, where $V_{ds} > V_{gs} - V_{th}$, as in Figure 3.

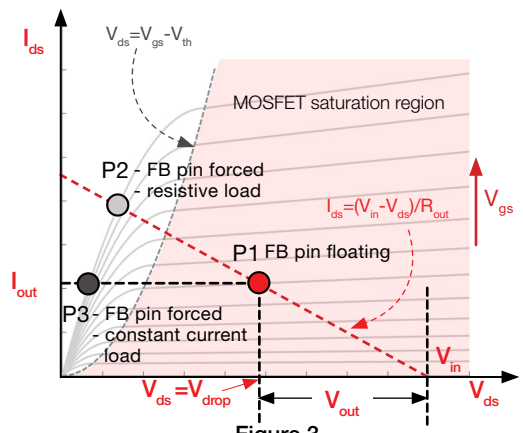


Figure 3

In the saturation region, the MOSFET drain-source current I_{ds} is given by equation (3):

(3) $$I_{ds} = \beta/2 \, (V_{gs} - V_{th})^2 \, [1 + \lambda \, (V_{ds} - (V_{gs} - V_{th}))]$$

where V_{th} is the gate-source threshold voltage, λ is the channel-length modulation factor, and the factor β depends on charge carriers mobility, channel width and length, and gate oxide capacitance per unit area. The grey curves of Figure 3 are the plots of equation (3) I_{ds} vs the drain-source voltage, for increasing values of the gate-source voltage, whereas the red dashed curve is the plot of equation (2). If the MOSFET operates in the saturation region, the feedback control has margin to adjust the gate-source voltage V_{gs} and find the value such that I_{ds} and V_{ds} fulfill both equations (2) and (3), even though V_{in} and I_{out} vary, thus ensuring that the output voltage V_{out} equals the desired value, and the drain-to-source current I_{ds} equals the desired load current I_{out}.

The output voltage can be regulated if the MOSFET operates in the ohmic region too, where $V_{ds} < V_{gs} - V_{th}$, as in Figure 4.

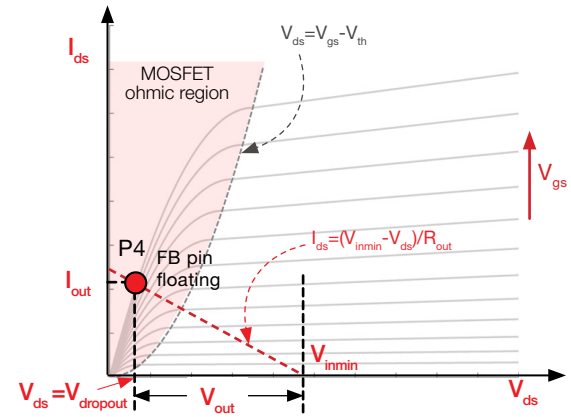


Figure 4

In the ohmic region, the MOSFET drain-source current I_{ds} is given by equation (4):

(4) $$I_{ds} = \beta \, (V_{gs} - V_{th} - V_{ds}/2) \, V_{ds}$$

The regulation in the ohmic region is achieved only if the input voltage is higher than the minimum value V_{inmin} for which there is a feasible value of gate-source voltage V_{gs} fulfilling both equations (2) and (3). In the ohmic region the drain-source voltage V_{ds} is very low and it is much smaller than $V_{gs} - V_{th}$, so that the drain-source current can be simplified as shown in equation (5):

(5) $$I_{ds} \approx V_{ds} / R_{ds,on}$$

where $R_{ds,on} = 1/[\beta \, (V_{gs} - V_{th})]$ is the MOSFET channel resistance. The channel resistance $R_{ds,on}$ provides a measure of the dropout voltage $V_{dropout} = V_{inmin} - V_{out}$.

Experiment set-up: configuration

The instruments needed for this experiment are: a DC POWER SUPPLY, a DC ELECTRONIC LOAD, four MULTIMETERS, and a SIGNAL GENERATOR. Figure 5 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

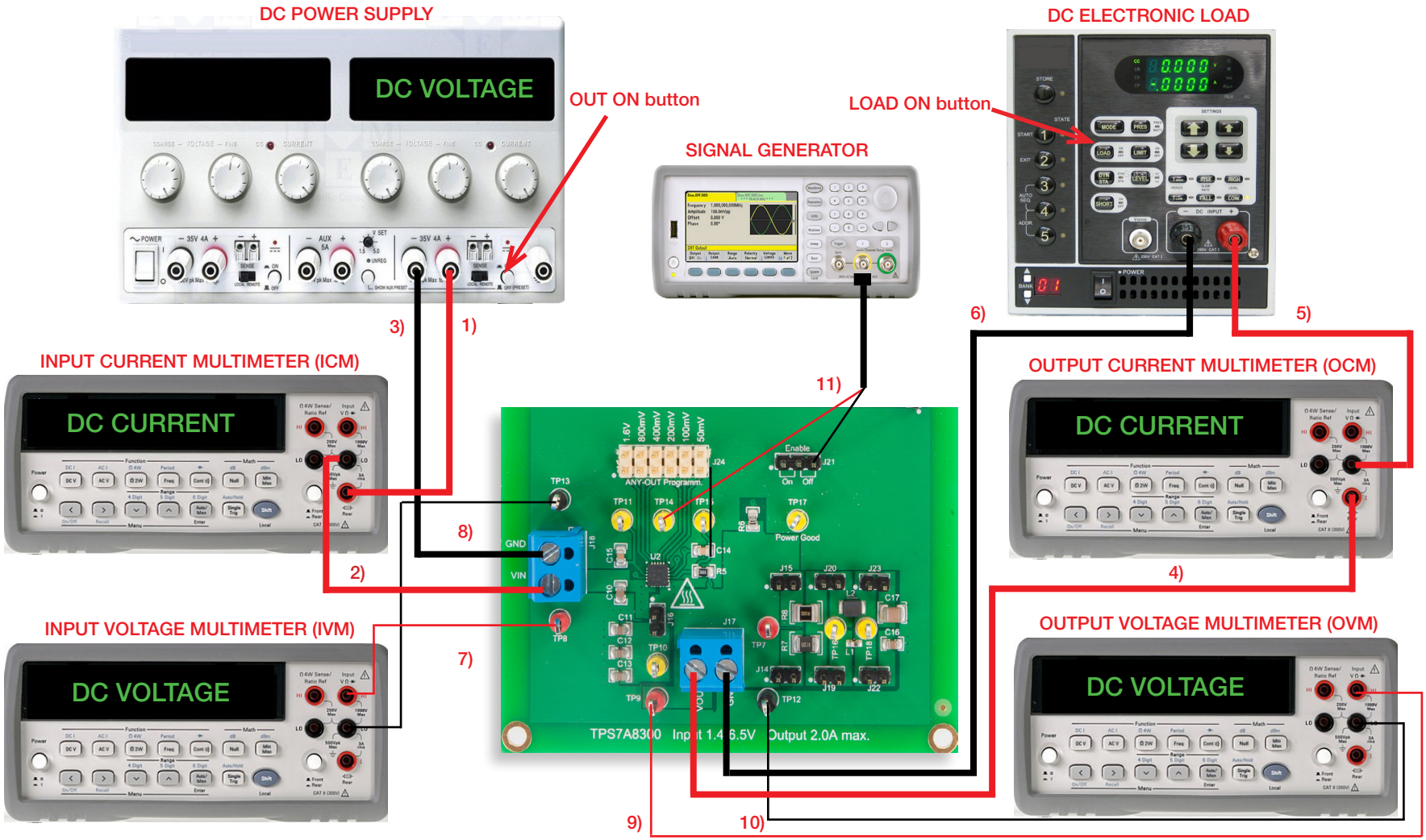


Figure 5. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the POSITIVE (RED) OUTPUT of the DC POWER SUPPLY to the POSITIVE (RED) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM)
[WARNING: the positive current input of the MULTIMETERS is distinguished from the positive voltage input]

2) connect the NEGATIVE (BLACK) CURRENT INPUT of the INPUT CURRENT MULTIMETER (ICM) to the INPUT (VIN) of the J_{18} screw terminal of the TPS7A8300 LDO regulator

3) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the GROUND (GND) of the J_{18} screw terminal of the TPS7A8300 LDO regulator

4) connect the OUTPUT (VOUT) of the J_{17} screw terminal of the TPS7A8300 LDO regulator to the POSITIVE (RED) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM)
[WARNING: the positive current input of the MULTIMETERS is distinguished from the positive voltage input]

5) connect the NEGATIVE (BLACK) CURRENT INPUT of the OUTPUT CURRENT MULTIMETER (OCM) to the POSITIVE (RED) INPUT of the ELECTRONIC LOAD

6) connect the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD to the GROUND (GND) of the J_{17} screw terminal of the TPS7A8300 LDO regulator

7) connect the POSITIVE (RED) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_8, which is the VIN of the TPS7A8300 LDO regulator

8) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the INPUT VOLTAGE MULTIMETER (IVM) to the TEST PIN TP_{13}, which is GND of the TPS7A8300 LDO regulator

9) connect the POSITIVE (RED) VOLTAGE INPUT of the OUPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_9, which is VOUT of the TPS7A8300 LDO regulator

10) connect the NEGATIVE (BLACK) VOLTAGE INPUT of the OUTPUT VOLTAGE MULTIMETER (OVM) to the TEST PIN TP_{12}, which is the GND of the TPS7A8300 LDO regulator

11) connect the POSITIVE terminal of the OUTPUT of the SIGNAL GENERATOR to TEST PIN TP_{14} of the TPS7A8300 LDO regulator and the GROUND terminal of the OUTPUT of the SIGNAL GENERATOR to the ground of the TPS7A8300 LDO regulator (use the J_{21} connected to ground, as shown in Figure 5)

Test#1: preparation and procedure

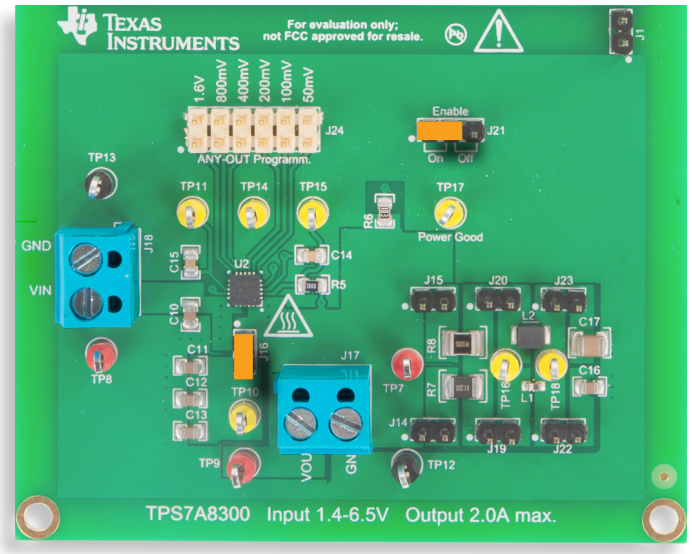


Figure 6. TPS7A8300 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 6):

- J_{21} **shorted** in **ON** position → LDO operation enabled
- J_{24} **open** → nominal output voltage V_{ou} = 0.8V
- J_{16} **shorted** → C_{11} - C_{13} (3x10μF) output capacitors connected
- J_{14} **AND** J_{15} **open** → R_7 (1mΩ) or R_8 (100mΩ) OUT resistors disconnected
- J_{19} **AND** J_{20} **open** → L_1 (1nH) or L_2 (100nH) output inductors disconnected
- J_{22} **AND** J_{23} **open** → C_{16} (10μF) or C_{17} (47μF) output capacitors disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤ 1A
3) set the OCM in DC CURRENT MODE, with range ≤ 1A
4) set the IVM in DC VOLTAGE MODE, with range ≤ 10V
5) set the OVM in DC VOLTAGE MODE, with range ≤ 1V
6) turn on the POWER SUPPLY, keep the "OUT ON" button OFF, set the voltage at 1.4V and the current limit at 1A
7) turn on the ELECTRONIC LOAD, keep the "LOAD ON" button OFF, set the CONSTANT CURRENT MODE, and set the current at 50mA
8) turn ON the SIGNAL GENERATOR, keep the "OUT ON" button OFF, set the DC MODE, set the output coupling at 1MΩ, and set the voltage at 775mV
9) turn ON the POWER SUPPLY "OUT ON" button. In these conditions you should read about 1.4V in the IVM display about 0.8V in the OVM display, about 0A in the OCM display and 0A in the ICM display (if you don't read these values, turn OFF the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps)
10) turn ON the ELECTRONIC LOAD ON button. In these conditions you should read about 1.4V in the IVM display, about 0.8V in the OVM display, 50mA in the OCM display and slightly more than 50mA in the ICM display (if you read values much different than the one listed above, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps)
11) measure the input and output voltages for the load current values listed in Table 1 (you do not need to turn OFF the ELECTRONIC LOAD "LOAD ON" button while varying the load current)
12) reset the load current at 50mA, turn ON the SIGNAL GENERATOR "OUT ON" button and repeat step 11)
13) turn OFF the SIGNAL GENERATOR "OUT ON" button, reset the load current at 50mA, set the POWER SUPPLY voltage at 2.5V, and repeat steps 11) -12)
14) at the end of the measurements, turn OFF the SIGNAL GENERATOR "OUT ON" button, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

1) Measure the output voltage in the operating conditions indicated in Table 1, calculate the difference between the input and the output voltage.
2) Calculate the equivalent MOSFET channel resistance $R_{ds,on} = (V_{in} - V_{out}) / I_{ds}$ with Test Pin TP_{14} voltage forced to 0.775V.
3) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in relevant references.

Table 1. Output voltage and dropout voltage of the TPS7A8300 LDO regulator at different load current and input voltage, with Test Pin TP_{14} voltage floating or forced at 0.775V

(1) V_{out} [V]	(2) $V_{drop} = V_{in} - V_{out}$ [mV]	I_{OUT} [mA]					
		50		250		500	
V_{in} = 1.4V	TP_{14} floating	(1)	(2)	(1)	(2)	(1)	(2)
	TP_{14} = 0.775V	(1)	(2)	(1)	(2)	(1)	(2)
	(3) $R_{ds,on}$ @ TP_{14} = 0.775V	(3)		(3)		(3)	
V_{in} = 2.5V	TP_{14} floating	(1)	(2)	(1)	(2)	(1)	(2)
	TP_{14} = 0.775V	(1)	(2)	(1)	(2)	(1)	(2)
	(3) $R_{ds,on}$ @ TP_{14} = 0.775V	(3)		(3)		(3)	

Output capacitors, resistors, inductors:

J_{16} connects the output capacitors C_{11} - C_{13} (3x10µF)

J_{14} connects the output resistor R_7 (1mΩ)
J_{15} connects the output resistor R_8 (100mΩ)

J_{19} connects the output inductor L_1 (1nH)
J_{20} connects the output inductor L_2 (100nH)

J_{22} connects the output capacitor C_{16} (10µF)
J_{23} connects the output capacitor C_{17} (47µF)

Answer:

1. Is the drop voltage V_{drop} lower with TP_{15} = 0.775V than with TP_{14} voltage floating? ☐ yes ☐ no ☐ it depends on: _____

2. How do the input voltage and load current influence the drop voltage and the channel resistance with TP_{14} voltage forced at 0.775V? _____

Test#2: preparation and procedure

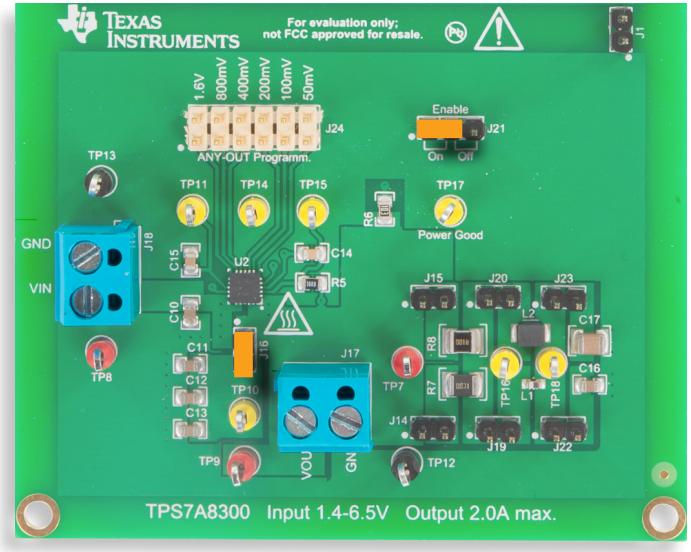


Figure 7. TPS7A8300 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 7):

- J_{21} **shorted** in **ON** position → LDO operation enabled
- J_{24} **open** → nominal output voltage V_{out} = 0.8V
- J_{16} **shorted** → C_{11}- C_{13} (3x10μF) output capacitors connected
- J_{14} **AND** J_{15} **open** → R_7 (1mΩ) and R_8 (100mΩ) output resistors disconnected
- J_{19} **AND** J_{20} **open** → L_1 (1nH) and L_2 (100nH) output inductors disconnected
- J_{22} **AND** J_{23} **open** → C_{16} (10μF) and C_{17} (47μF) output capacitors disconnected

Test Procedure:

1) turn on the MULTIMETERS
2) set the ICM in DC CURRENT MODE, with range ≤1A
3) set the OCM in DC CURRENT MODE, with range ≤1A
4) set the IVM in DC VOLTAGE MODE, with range ≤10V
5) set the OVM in DC VOLTAGE MODE, with range ≤1V
6) turn on the POWER SUPPLY, keep the “OUT ON” button OFF, set the voltage at 1.4V and the current limit at 1A
7) turn on the ELECTRONIC LOAD, keep the “LOAD ON” button OFF, set the CONSTANT CURRENT MODE, and set the current at 50mA
8) turn ON the POWER SUPPLY “OUT ON” button. In these conditions you should read about 1.4V in the IVM display, about 0.8V in the OVM display, about 0A in the OCM display and 0A in the ICM display (if you don’t read these values, turn OFF the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
9) turn ON the ELECTRONIC LOAD ON button. In these conditions you should read about 1.4V in the IVM display, about 0.8V in the OVM display, 50mA in the OCM display and slightly more than 50mA in the ICM display (if you read values much different than the one listed above, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY and verify the previous steps)
10) measure the input and output currents for the line voltage and load current values listed in Table 2 (you do not need to turn OFF the ELECTRONIC LOAD “LOAD ON” button and the POWER SUPPLY “OUT ON” button while varying the load current and line voltage)
11) at the end of the measurements, turn OFF the SIGNAL GENERATOR “OUT ON” button, turn OFF the “LOAD ON” button of the ELECTRONIC LOAD and the “OUT ON” button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) Measure the input current I_{in} and output current I_{out}, and calculate the ground current I_{GND} in the operating conditions listed in the Table 2.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in relevant references.

Table 2. Input and ground current of the TPS7A8300 LDO regulator at different load current and input voltage

(1) I_{in} [mA]	V_{in} [V]					
(2) $I_{GND} = I_{in} - I_{out}$ [mA]	1.4	1.8	2.2	2.6	3.0	3.2
I_{OUT} = 50mA	(1)	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)	(2)
I_{OUT} = 250mA	(1)	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)	(2)
I_{OUT} = 500mA	(1)	(1)	(1)	(1)	(1)	(1)
	(2)	(2)	(2)	(2)	(2)	(2)

Output capacitors, resistors, inductors:

J_{16} connects the output capacitors C_{11}- C_{13} (3x10µF)

J_{14} connects the output resistor R_7 (1mΩ)

J_{15} connects the output resistor R_8 (100mΩ)

J_{19} connects the output inductor L_1 (1nH)

J_{20} connects the output inductor L_2 (100nH)

J_{22} connects the output capacitor C_{16} (10µF)

J_{23} connects the output capacitor C_{17} (47µF)

Answer:

1. How does the I_{GND} current change when the input voltage increases? ☐ increases ☐ decreases ☐ other: _____

2. How does the I_{GND} current change when the load current increases? ☐ increases ☐ decreases ☐ other: _____

Discussion

In Test#1 we are interested in investigating the dropout voltage of the LDO regulator, observing the operation of the N-channel MOSFET pass device in the ohmic region (dropout) and calculating the MOSFET channel resistance.

With the FB pin floating, the TPS7A8300 LDO regulator drives the operating point of the MOSFET pass device in the saturation region (e.g. point P_1 of Figure 3) or in the ohmic region (e.g. point P_4 of Figure 4) to regulate the output voltage. Regulation is achieved provided that the difference between the input voltage and the output voltage is greater than the MOSFET pass device dropout voltage. In *Experiment 1* we measure the value of the dropout voltage of the TPS7A4901 LDO regulator by decreasing the input voltage until the output voltage regulation is lost. In this experiment, instead, we fix the input voltage and we force the FB pin voltage to a value lower than the reference voltage. This way, we emulate the effect of having an output voltage lower than the nominal value, and then we induce the feedback controller to increase the MOSFET gate-source voltage, up to the maximum value V_{gsmax} allowed by the internal MOSFET driver, trying to reduce the drain-source voltage to maintain the output voltage regulation. In *Experiment 1* we observed a decrease of the output voltage due to the decrease of the input voltage below the minimum value determined by the dropout voltage of the pass device, whereas in this experiment we observe an increase of the output voltage due to the decrease of the pass device voltage at its dropout value determined by the external voltage clamp imposed on the FB pin. The dropout voltage measured with this technique depends on the type of load. In fact, when the FB pin voltage is clamped, the MOSFET operating point may be forced to point P_2 or to point P_3 of Figure 3, depending on whether the load is a resistor or a constant current load (like the electronic load used for the test), respectively. The operating point P_2 involves a higher value of the dropout voltage corresponding to a higher value of the load current. The MOSFET channel resistance measured in the two points P_2 and P_3 is almost the same, as they stay on the same I_{ds} vs V_{ds} curve corresponding to the maximum gate-source voltage V_{gsmax} of the MOSFET driver. The output voltage is not regulated when the pass device operates in point P_2 or in point P_3: in both cases the output voltage V_{out} value is given by the input voltage minus the dropout voltage, $V_{out} = V_{in} - V_{dropout}$. Given the input voltage, if the load current increases, the operating points P_2 and P_3 move upward rightside, thus yielding a higher dropout voltage. Given the load current, if the input voltage increases, the operating point P_2 moves upward rightside, thus providing a higher dropout voltage, whereas point P_3 is in theory insensitive, thus providing the same dropout voltage. The channel resistance $R_{ds,on} = 1 / [\beta (V_{gs} - V_{th})]$ we measure by forcing the MOSFET to operate on the I_{ds} vs V_{ds} curve corresponding to the maximum gate-source voltage V_{gsmax} of the MOSFET driver may increase at higher current. In fact, an increase of the current involves higher ohmic losses and then a higher junction temperature, with consequent decrease of the parameters β and V_{th} which decrease at higher temperature. The channel resistance is expected to increase at higher input voltage, which involves a higher dropout voltage.

In Test#2 we are interested in investigating the correlations aming the ground current of the LDO regulator and the values of the load current and input voltage.

The ground current I_{gnd}, also called quiescent current, is the difference between the LDO regulator input and output currents, and consists of several components determined by the band-gap reference, the sensing resistors, the error amplifier, and the pass device drive current, which do not contribute to output power. A lower ground current improves the regulator efficiency, as shown in *Experiment 2*. The ground current is highly influenced by the type of series pass element and its junction temperature. In *Experiment 2* it is shown that the ground current I_{gnd} of TPS7A4901 LDO regulator is heavily dependent on the load current. This is caused by the inherent nature of the PNP bipolar transistor, which is a current-driven device, whose base current is merely proportional to the collector current and is permanently sinked to gound. The N-channel MOSFET pass device of the TPS7A8300 LDO regulator is a voltage-driven device (it could also be classified as charge-driven device) and a higher load current involves a higher gate-source voltage V_{gs}. In steady state conditions the MOSFET gate current is almost zero. The slight increase of the ground current observed at higher load current is mainly caused by the error amplifier, which provides the higher gate-source voltage needed for the MOSFET to conduct a higher current, as you may observe in Figure 3. The ground current of the TPS7A8300 LDO regulator is, instead, differently sensitive to the input voltage, as it can be realized looking at Fugure 3. In particular, when the input voltage is not near the mimimum value determined by the MOSFET dropout voltage, the sensitivity is higher as the MOSFET likely operates in the ohmic region, where the gate-source voltage V_{gs} needed to deliver a certain load current is strongly varying with the drain-source voltage V_{ds}. When the input voltage is high enough to determine the MOSFET operation in the saturation region, the ground current is almost insensitive to the input voltage, as in the saturation region the I_{ds} vs V_{ds} curve is almost flat.

Experimental plots

The plots collected in these pages are samples of experimental measurements performed on the TPS7A8300 LDO regulator. They show the droupout voltage and the ground current of the LDO regulator for different input voltage, load current and junction temperature (*see [3] for further details*).

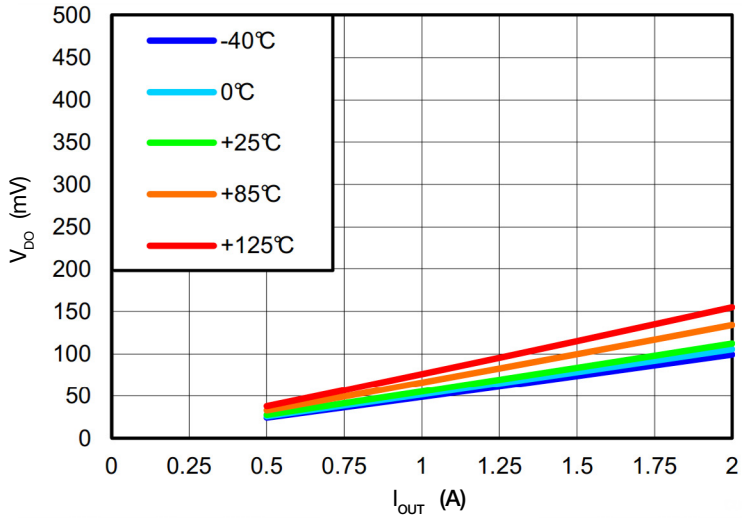


Figure 8. TPS7A8300 LDO regulator droupout voltage vs output current for: V_{out}=0.8V and V_{in}=1.4V

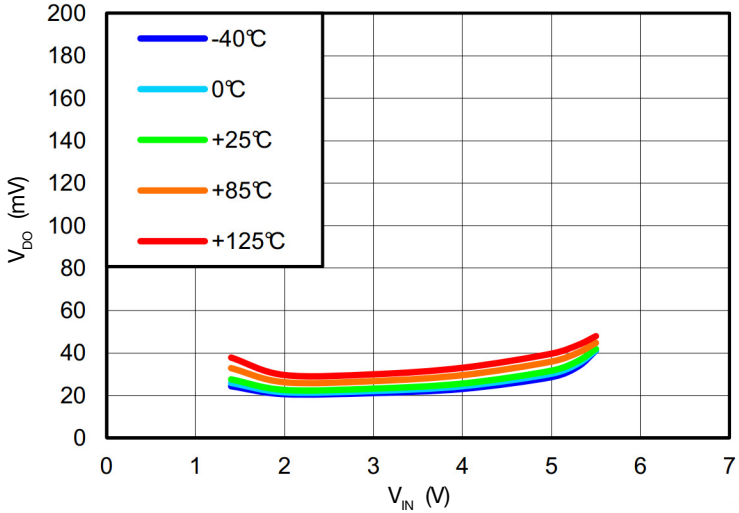


Figure 9. TPS7A8300 LDO regulator droupout voltage vs input voltage for: V_{out}=0.8V and I_{out}=0.5A

The plots of Figures 8 and 9 highlight the influence of the load current and of the input voltage on the droupout voltage of the TPS7A8300 LDO discussed in the previous section.

Experimental plots

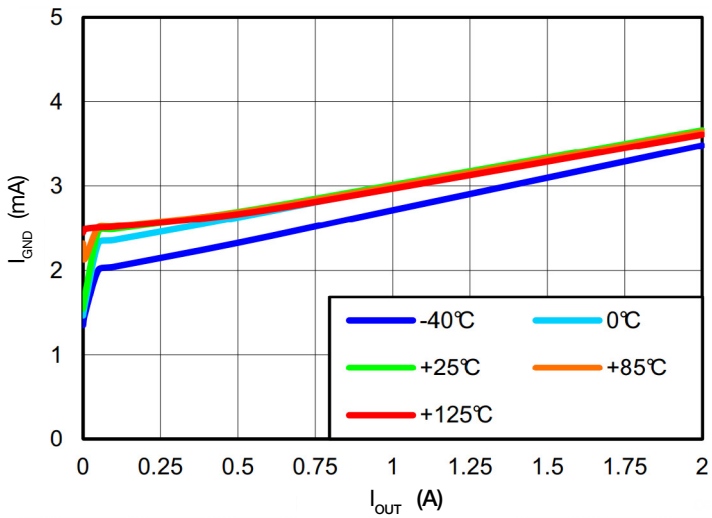


Figure 10. TPS7A8300 LDO regulator ground current vs output current for: V_{out}=0.8V and V_{in}=1.4V

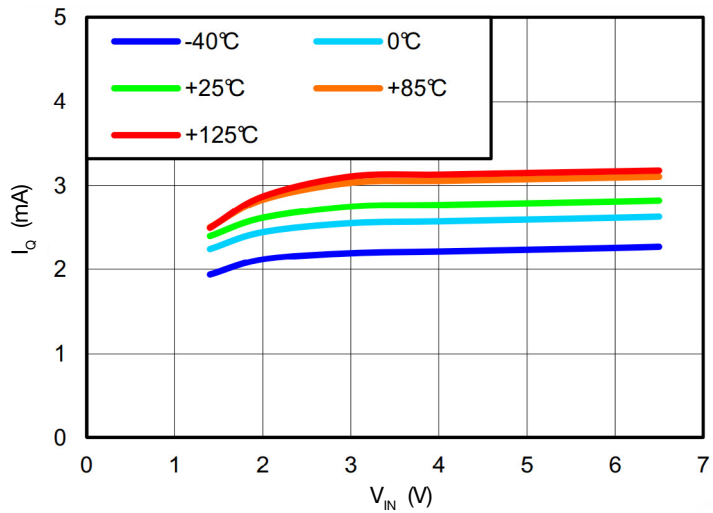


Figure 11. TPS7A8300 LDO regulator quiescent current vs input voltage for: V_{out}=0.8V and I_{out}=5mA

The plots of Figures 10 and 11 highlight the influence of the load current and of the input voltage on the ground current of the TPS7A8300 LDO discussed in the previous section.

Experiment 6

The goal of this experiment is to analyze how the characteristics of the output capacitor influence the load-transient waveform of an LDO regulator. The TPS7A8300 LDO regulator is used for this experiment.

Case Study

The goal of this experiment is to analyze how the output voltage load transient surges of the LDO regulator depend on the output capacitor.

The subject of investigation in this experiment is the impact of the output capacitor characteristis on the waveform of the LDO regulator output voltage during load-transients. A simplified schematic of the TPS7A8300 LDO regulator is shown in Figure 1. The combination of output capacitance C_{out}, resistance ESR and inductance ESL influences the load transient response of the regulator, as they influence the LDO regulator voltage loop gain, as discussed in *Experiment 3*. A good load transient response is characterized by small voltage surges, short settling time and absence of oscillations. The global output R-L-C combination is determined by the inherent R-L-C characteristics of the output capacitor in itself, and by the parasitic inductances and resistances of the Printed Circuit Board (PCB) layout traces. The group of components R_7, R_8, L_1, L_2, C_{16} and C_{17} mounted in the output section of the TPS7A8300 LDO regulator board allows to emulate an equivalent output capacitor with different combinations of capacitance C_{out}, resistance ESR and inductance ESL.

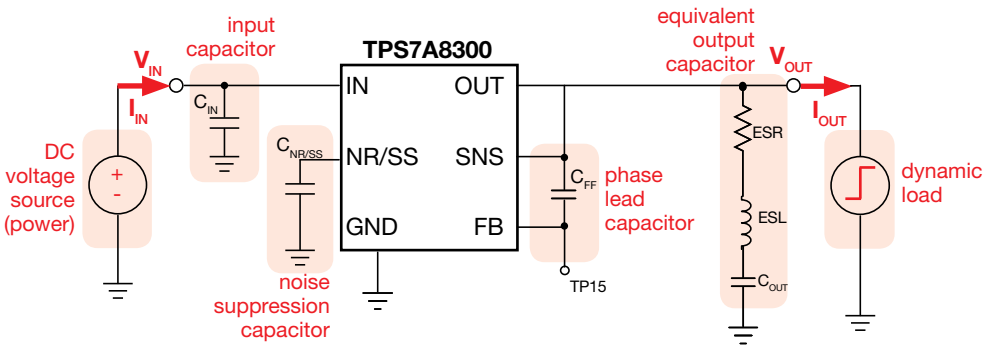


Figure 1. Simplified schematic of the TPS7A8300 LDO regulator

Test#1. We connect the LDO regulator output to an electronic load operating in dynamic mode with an AC 750mAp-p, 100Hz square wave component added to a 250mA DC component, and measure:
- the magnitude of output voltage surge overshoots and undershoots, $\Delta V_{out,over}$ and $\Delta V_{out,under}$;
- the time $t_{pk,over}$ from the instant where the load step-down starts to the time where the output voltage shows obvershoot;
- the time $t_{pk,under}$ from the instant where the load step-up starts to the time where the output voltage shows undershoot;
- the settling times $t_{set,over}$ and $t_{set,under}$ where the output voltage settles to +/- 10% of the regulated output.

Test#2. We use the additional components available on the output section of the TPS7A8300 LDO regulator board to emulate different combinations of R-L-C characteristics and measure the output voltage surge peaks, to observe the effect of ESL, ESR and C_{out} in combination with different slew-rate level of the dynamic load current.

Theory Background

The fundamentals of output capacitor impact on load transient response are provided in this section *(see [1][4][11][12] for a general discussion of LDO regulators operation, [3] for more details on TPS7A8300 operation and features, and refer to Experiment 3 for discussion of loop gain impact on load transient reponse of LDO regulators).*

Figure 2 shows the model of a capacitor, including the capacitance C_{out} the equivalent series resistance ESR and inductance ESL.

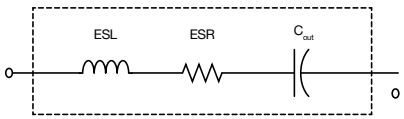


Figure 2

The values of ESL and ESR depend on the type of device. For a given capacitance C_{out}, the ESR and ESL of ceramic capacitors are very small whereas they are much bigger in electrolytic capacitors. Figure 3 shows an ideal qualitative plot of the LDO load transient response, including the effects of the parameters C_{out}, ESR and ESL.

The effect of capacitance C_{out} is shown in Figure 4. An LDO cannot adjust the pass device current to instantly track fast load transients. The time the LDO takes to respond is determined by the setup of its feedback loop. During this time, the output capacitor supplies the current difference between the pass device and load. With an output capacitor having very low ESR and ESL, increasing the capacitance C_{out} increases the LDO response time and decreases the voltage surges magnitude, as a higher capacitance reduces the loop gain bandwidth but at the same time determines a smaller voltage variation as a consequence of the charge delivered to load.

The effect of the ESL is shown in Figure 5. During the rising edge of the load current, the ESL determines a voltage spike of magnitude V_{ESL}= ESL $\Delta I_{OUT}/\Delta t$, increasing with the ESL value and with the load transient slew rate $\Delta I_{OUT}/\Delta t$. The parasitic inductances of PCB traces add up to the ESL. A larger V_{ESL} generates a stronger error amplifier response and then a faster LDO response, but a too high V_{ESL} yields undesired noise. A good layout design and the placement of the output capacitor as close as possible to the LDO out pin are necessary to keep the effects of the total ESL during load transients acceptable.

The effect of the ESR is shown in Figure 6. During the rising edge of the load current, the ESR determines a voltage ramp of magnitude V_{ESR} = ESR ΔI_{OUT}, increasing with the load transient step magnitude ΔI_{OUT} and with the ESR value. A larger V_{ESR} generates a stronger error amplifier response and then a faster LDO response, but a too high V_{ESR} yields undesired noise and a too big ESR may cause instability, as the ESR also contributes a zero in the loop gain. There is a trade-off based on ESR value, between stability and fast transient response.

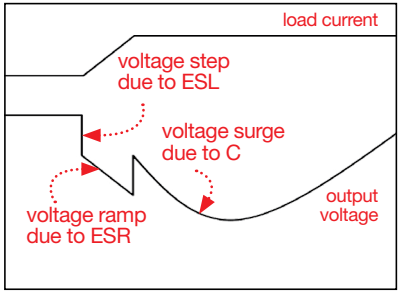


Figure 3

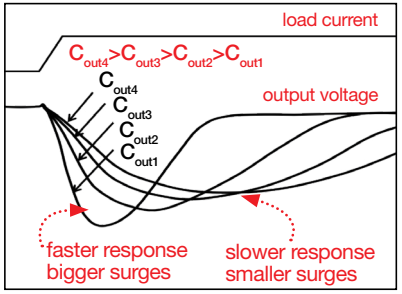


Figure 4

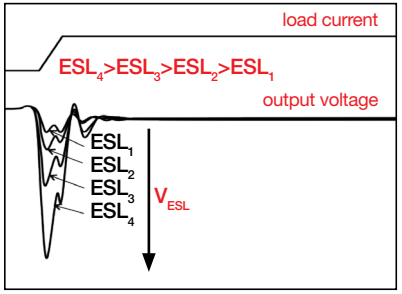


Figure 5

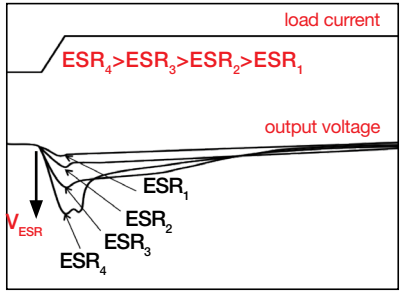


Figure 6

Experiment set-up: configuration

The instruments needed for this experiment are: a DC POWER SUPPLY, a DC ELECTRONIC LOAD with dynamic current mode feature, and an OSCILLOSCOPE. Figure 7 shows the instruments connections. Follow the instructions provided in next page to set-up the connections.

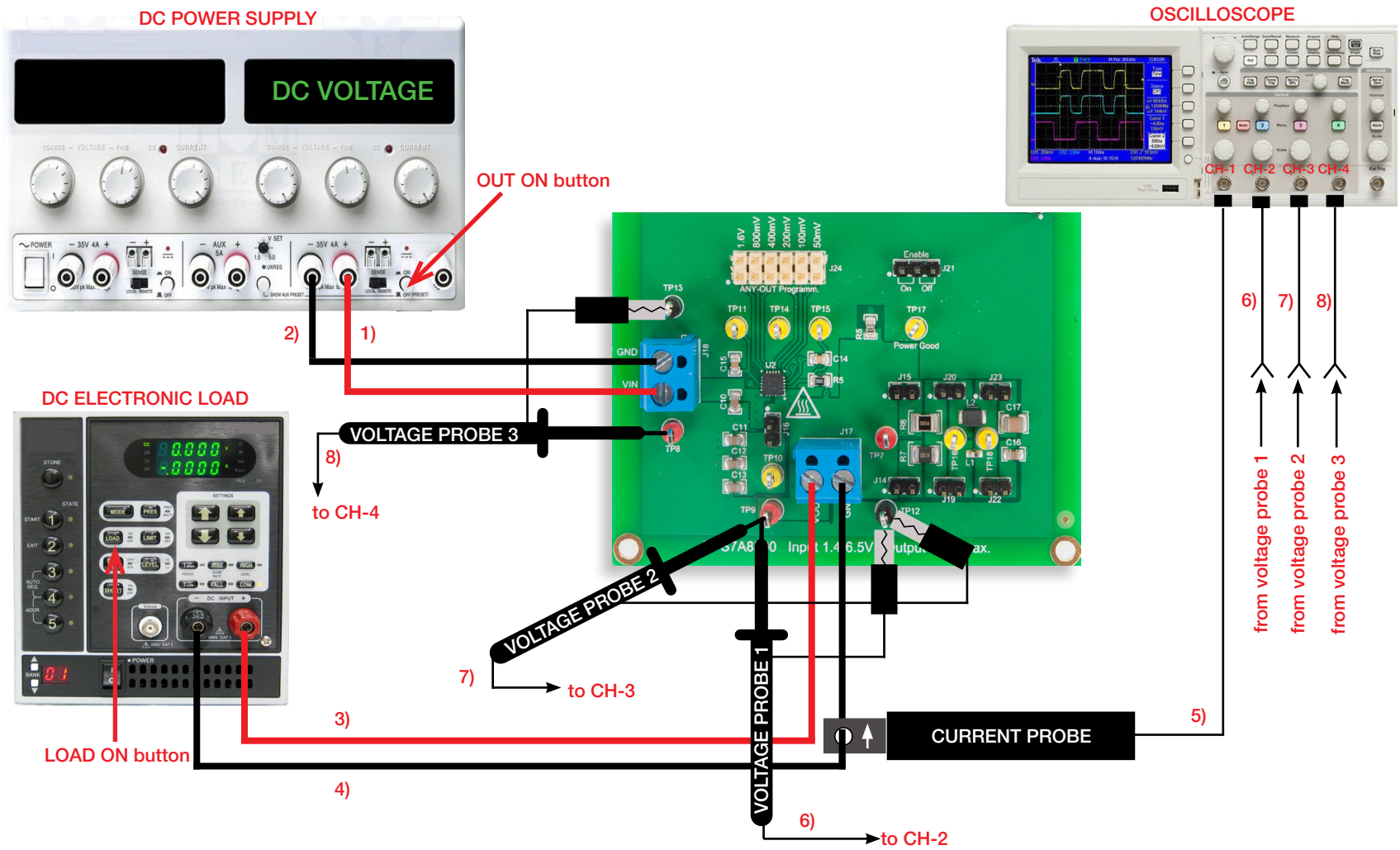


Figure 7. Experiment set-up.

Experiment set-up: instructions

With all the instruments turned off, make the following connections:

1) connect the POSITIVE (RED) OUTPUT of the DC POWER SUPPLY to the INPUT (VIN) of the J_{18} screw terminal of the TPS7A8300 LDO regulator

2) connect the NEGATIVE (BLACK) OUTPUT of the DC POWER SUPPLY to the GROUND (GND) of the J_{18} screw terminal of the TPS7A8300 LDO regulator

3) connect the OUTPUT (VOUT) of the J_{17} screw terminal of the TPS7A8300 LDO regulator to the POSITIVE (RED) CURRENT INPUT of the ELECTRONIC LOAD

4) connect the GROUND (GND) of the J_{17} screw terminal of the TPS7A8300 LDO regulator to the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD

5) connect a current probe to channel 1 of the OSCILLOSCOPE and hang it on the cable connecting the GROUND (GND) of the J_{17} screw terminal of the TPS7A8300 LDO regulator to the NEGATIVE (BLACK) INPUT of the ELECTRONIC LOAD, ensuring that the arrow printed on the probe clamps corresponds to the current that exits the ELECTRONIC LOAD

6) connect a voltage probe to channel 2 of the OSCILLOSCOPE and hang it to TEST PIN TP_9, which is the output voltage of the TPS7A8300 LDO regulator
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

7) connect a voltage probe to channel 3 of the OSCILLOSCOPE and hang it to TEST PIN TP_9, which is the output voltage of the TPS7A8300 LDO regulator
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

8) connect a voltage probe to channel 4 of the OSCILLOSCOPE and hang it to TEST PIN TP_8, which is the input voltage of the TPS7A8300 LDO regulator
[WARNING: **DO NOT INVERT** the positive and ground connections of the voltage probe]

Test#1: preparation and procedure

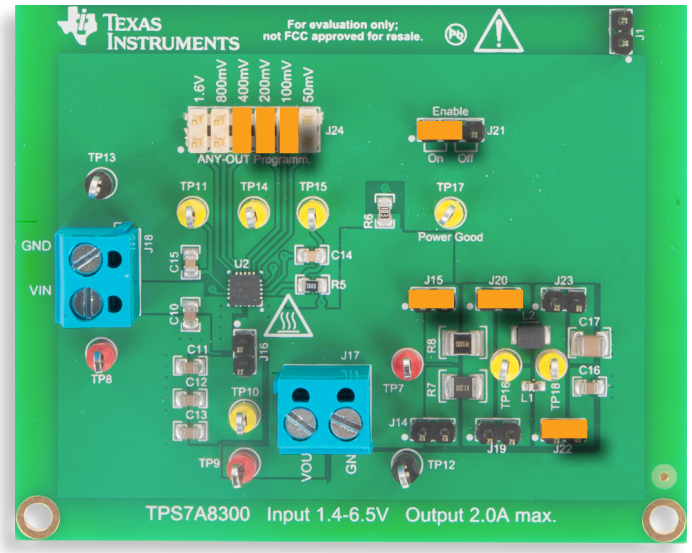


Figure 8. TPS7A8300 LDO board: jumpers set-up for Test#1

Jumpers set-up (see Figure 8):

- J_{21} **shorted** in **ON** position → LDO operation enabled
- J_{24} **shorted** (with labels 100mV, 200mV and 400mV) → nominal output voltage V_{out} = 1.5V
- J_{15} **shorted** → R_8 (100mΩ) output resistor connected
- J_{20} **shorted** → L_2 (100nH) output inductor connected
- J_{22} **shorted** → C_{16} (10μF) output capacitor connected
- J_{16} **open** → C_{11}-C_{13} (3x10μF) output capacitors disconnected
- J_{14} **open** → R_7 (1mΩ) output resistor disconnected
- J_{19} **open** → L_1 (1nH) output inductor disconnected
- J_{23} **open** → C_{17} (47μF) output capacitor disconnected

Test Procedure:

1) turn on the OSCILLOSCOPE, set CH-1 in DC 50Ω coupling mode, select CH-1 as trigger source, set CH-2 in DC 1MΩ coupling mode, set CH-3 in AC 1MΩ coupling mode, set CH-4 in DC 1MΩ coupling mode, and execute the "degauss" of the current probe to remove dc bias
2) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the voltage at 2.5V, and set the CURRENT LIMIT at 1.5A
3) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the dynamic current MODE and fix:
   - low current level at 100mA and low current time at 10ms
   - high current level at 1A and high current time at 10ms
   - current rise and fall slew-rates at the highest level allowed by the instrument
4) turn ON the POWER SUPPLY "OUT ON" button. In these conditions you should see on the OSCILLOSCOPE the traces of CH-1 (load current) and CH-3 (AC component of output voltage) as flat horizontal lines at 0 level, the trace of CH-2 (full output voltage) as a flat line at 1.5V level, and the trace of CH-4 (input voltage) as a flat line at 2.5V level
5) use OSCILLOSCOPE cursors (or measurement functions) to verify the values of the average input and output voltages. If you read value much different than the expected ones, turn OFF the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps
6) turn ON the ELECTRONIC LOAD "LOAD ON" button. In these conditions you should see CH-1 trace as a square-wave, CH-2 trace as a flat line with 1.5V average value, CH-3 trace as a flat line with 0V average value and small magnitude spikes of short duration in correspondence of load current transients, and CH-4 trace as a flat line at 2.5V level (see the experimental figures samples at the end of the experiment). Adjust the OSCILLOSCOPE setup to make the waveforms best fitting the scope width and height. Set the trigger level at 50% of the CH-1 trace
7) use the OSCILLOSCOPE measurement features to read the magnitudes of output voltage surges $\Delta V_{out,over}$ and $\Delta V_{out,under}$, the times $t_{pk,over}$ and $t_{pk,under}$ where $\Delta V_{out,over}$ and $\Delta V_{out,under}$ occur, and the settling times $t_{set,over}$ and $t_{set,under}$, on the CH-3 trace
8) turn OFF the ELECTRONIC LOAD "LOAD ON" button, turn OFF the POWER SUPPLY "OUT ON" button; setup the jumpers as indicated in section (b) of Table 1, turn ON the power supply "OUT ON" button, turn ON the ELECTRONIC LOAD "LOAD ON" button and repeat the step 7)
9) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#1: measure and calculate

1) Measure the magnitudes of output voltage surges $\Delta V_{out,over}$ and $\Delta V_{out,under}$, the times $t_{pk,over}$ and $t_{pk,\ under}$ where $\Delta V_{out,over}$ and $\Delta V_{out,under}$ occur, and the settling times $t_{set,over}$ and $t_{set,under}$ in the operating conditions indicated in Table 1.
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in relevant references.

Table 1. Output voltage surges, peak times and settling times of the TPS7A8300 LDO regulator during load transients, with different output capacitor, resistor and inductor setup, and maximum current slew-rate allowed by the electronic load in dynamic mode operation, for V_{in} = 2.5V and V_{out} = 1.5V

		I_{OUT} : 1A→100mA		I_{OUT} : 100mA→1A	
(a)	J_{14} op , J_{15} sh J_{19} op , J_{20} sh J_{22} sh , J_{23} op	(1) $\Delta V_{OUT,over}$ [mV]	(1)	(1) $\Delta V_{OUT,under}$ [mV]	(1)
		(2) $t_{pk,over}$ [ms]	(2)	(2) $t_{pk,under}$ [ms]	(2)
		(3) $t_{set,over}$ [ms]	(3)	(3) $t_{set,under}$ [ms]	(3)
(b)	J_{14} sh , J_{15} op J_{19} sh , J_{20} op J_{22} op , J_{23} sh	I_{OUT} : 1A→100mA		I_{OUT} : 100mA→1A	
		(1) $\Delta V_{OUT,over}$ [mV]	(1)	(1) $\Delta V_{OUT,under}$ [mV]	(1)
		(2) $t_{pk,over}$ [ms]	(2)	(2) $t_{pk,under}$ [ms]	(2)
		(3) $t_{set,over}$ [ms]	(3)	(3) $t_{set,under}$ [ms]	(3)

Output capacitors, resistors, inductors:

J_{16} connects the output capacitors C_{11}- C_{13} (3x10µF)

J_{14} connects the output resistor R_7 (1mΩ)
J_{15} connects the output resistor R_8 (100mΩ)

J_{19} connects the output inductor L_1 (1nH)
J_{20} connects the output inductor L_2 (100nH)

J_{22} connects the output capacitor C_{16} (10µF)
J_{23} connects the output capacitor C_{17} (47µF)

Answer:

1. Are the surges magnitude bigger for case (a) or for case (b) ? ☐ (a) ☐ (b) ☐ same ☐ it depends on: _____
2. Are the surges peak time shorter for case (a) or for case (b) ? ☐ (a) ☐ (b) ☐ same ☐ it depends on: _____
3. Is the settling time shorter for case (a) or for case (b) ? ☐ (a) ☐ (b) ☐ same ☐ it depends on: _____

Test#2: preparation and procedure

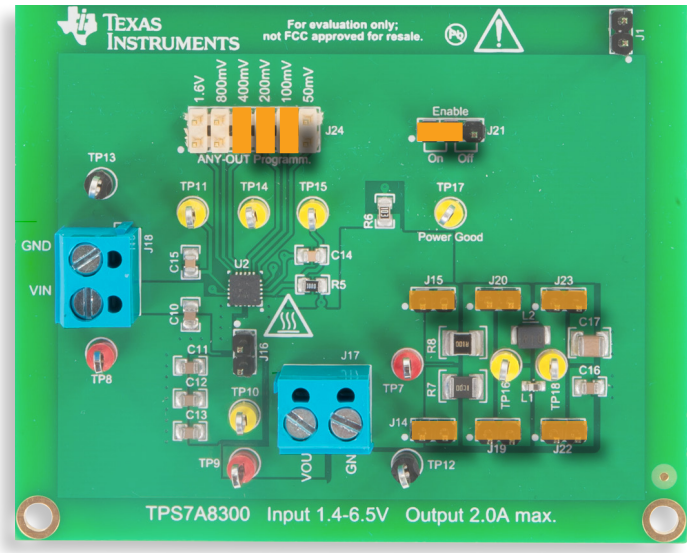


Figure 9. TPS7A8300 LDO board: jumpers set-up for Test#2

Jumpers set-up (see Figure 9):

- J_{21} **shorted** in **ON** position → LDO operation enabled
- J_{24} **shorted** (with labels 100mV, 200mV and 400mV) → nominal output voltage V_{out} = 1.5V
- J_{16} **open** → C_{11} - C_{13} (3x10μF) output capacitors disconnected
- J_{14} **OR** J_{15} **shorted** (*) → R_7 (1mΩ) or R_8 (100mΩ) output resistors connected
- J_{19} **OR** J_{20} **shorted** (*) → L_1 (1nH) or L_2 (100nH) output inductors connected
- J_{22} **OR** J_{23} **shorted** (*) → C_{16} (10μF) or C_{17} (47μF) output capacitors connected

[(*) WARNING: **at least one of the two jumpers MUST be connected**]

Test Procedure:

1) turn on the OSCILLOSCOPE, set CH-1 in DC 50Ω coupling mode, select CH-1 as trigger source, set CH-2 in DC 1MΩ coupling mode, set CH-3 in AC 1MΩ coupling mode, set CH-4 in DC 1MΩ coupling mode, and execute the "degauss" of the current probe to remove dc bias
2) turn on the POWER SUPPLY (ensure that the "OUT ON" button is OFF), set the voltage at 2.5V, and set the CURRENT LIMIT at 1.5A
3) turn on the ELECTRONIC LOAD (ensure that the "LOAD ON" button is OFF), set the dynamic current MODE and fix:
   - low current level at 100mA and low current time at 10ms
   - high current level at 1A and high current time at 10ms
   - current rise and fall slew-rates at the highest level allowed by the instrument
4) turn ON the POWER SUPPLY "OUT ON" button. In these conditions you should see on the OSCILLOSCOPE the traces of CH-1 (load current) and CH-3 (AC component of output voltage) as flat horizontal lines at 0 level, the trace of CH-2 (full output voltage) as a flat line at 1.5V level, and the trace of CH-4 (input voltage) as a flat line at 2.5V level
5) use OSCILLOSCOPE cursors (or measurement functions) to verify the values of the average input and output voltages. If you read value much different than the expected ones, turn OFF the "OUT ON" button of the DC POWER SUPPLY and verify the previous steps
6) turn ON the ELECTRONIC "LOAD ON" button. In these conditions you should see CH-1 trace as a square-wave, CH-2 trace as a flat line with 1.5V average value, CH-3 trace as a flat line with 0V average value and small magnitude spikes of short duration in correspondence of load current transients, and CH-4 trace as a flat line at 2.5V level (see the experimental figures samples at the end of the experiment). Adjust the OSCILLOSCOPE setup to make the waveforms best fitting the scope width and height. Set the trigger level at 50% of the CH-1 trace
7) select four different jumpers set-up for the equivalent output capacitor (see the WARNINGS in Test Preparation Section) and read the magnitude of output voltage surges $\Delta V_{out,over}$ with the different setup of the ELECTRONIC LOAD current slew-rate listed in Table 2 [WARNING: turn OFF the ELECTRONIC LOAD "LOAD ON" button first, and then turn OFF the POWER SUPPLY "OUT ON" button before changing the jumpers set-up; then, turn ON the POWER SUPPLY "OUT ON" button and finally the ELECTRONIC LOAD "LOAD ON" button]
8) at the end of the measurements, turn OFF the "LOAD ON" button of the ELECTRONIC LOAD and the "OUT ON" button of the DC POWER SUPPLY, then switch off all the instruments

Test#2: measure and calculate

1) Measure the magnitudes of output voltage surges $\Delta V_{out,over}$ with four different setup of the jumpers J_{14}, J_{15}, J_{19}, J_{20}, J_{22}, J_{23} and report the results in Table 2 [**NOTE:** according to the **WARNING** provided in the *Test Preparation*, you have to ensure that there is a path from the output voltage node to the ground node through R_7 or R_8, L_1 or L_2, and C_{16} or C_{17}].
2) Answer the questions and try to motivate the results of your observation based on the information provided in the *Theory Background* section and in relevant references.

Table 2. Output voltage surges of the TPS7A8300 LDO regulator during load transients, with different output capacitor, resistor and inductor setup, for V_{in} = 2.5V and V_{out} = 1.5V

load current slew/rate	setup#1: _____		setup#2: _____		setup#3: _____		setup#4: _____	
(1) 0.01 A/µs	$\Delta V_{out,over}$ [mV]	(1)	$\Delta V_{out,over}$ [mV]	(1)	$\Delta V_{out,over}$ [mV]	(1)	$\Delta V_{out,over}$ [mV]	(1)
(2) 0.1 A/µs		(2)		(2)		(2)		(2)
(3) 1.0 A/µs		(3)		(3)		(3)		(3)
	ESR [mΩ]		**ESR** [mΩ]		**ESR** [mΩ]		**ESR** [mΩ]	
	ESL [nH]		**ESL** [nH]		**ESL** [nH]		**ESL** [nH]	
	C_{out} [µF]		C_{out} [µF]		C_{out} [µF]		C_{out} [µF]	

Output capacitors, resistors, inductors:

J_{16} connects the output capacitors C_{11}- C_{13} (3x10µF)

J_{14} connects the output resistor R_7 (1mΩ)
J_{15} connects the output resistor R_8 (100mΩ)

J_{19} connects the output inductor L_1 (1nH)
J_{20} connects the output inductor L_2 (100nH)

J_{22} connects the output capacitor C_{16} (10µF)
J_{23} connects the output capacitor C_{17} (47µF)

Answer:

1. What is the output setup determining the minimum magnitude of output voltage surge $\Delta V_{OUTover}$? ☐ #1 ☐ #2 ☐ #3 ☐ #4

   motivation: _____

2. What is the output setup determining the maximum magnitude of output voltage surge $\Delta V_{OUTover}$? ☐ #1 ☐ #2 ☐ #3 ☐ #4

   motivation: _____

Discussion

In Test#1 we are interested in investigating correlations between the load transient response of the TPS7A8300 LDO regulator and the characteristics of the equivalent output capacitor.

In *Experiment 3* it is highlighted that the load transient response of an LDO regulator is determined by the feedback loop gain and by the characteristics of the output capacitor. The TPS7A8300 LDO regulator has an internal compensation setup ensuring a cross-over frequency that can range from tens of kHz to MHz as load current rises from few mAs up to 2A. If the electronic load is not able to impose a very-high slew-rate to the dynamic load current, then the load transient overshoot and undershoot observed in the output voltage are determined by the loop gain. Therefore, the influence of the output capacitor characteristics on the load transient in these conditions depends on the effect produced by the output capacitor itself on the loop gain. As discussed in *Experiment 3*, a higher output capacitance determines a lower frequency of the loop gain pole $\omega_{Pload} = I_{OUT}/(C_{OUT}V_{OUT})$, thus decreasing the cross-over frequency and determining higher magnitude and slower overshoots/undershoots. Moreover, a higher ESR reduces the frequency of the loop gain zeo $\omega_Z = 1/(C_{OUT}ESR)$, thus increasing the cross-over frequency and determining faster overshoots/undershoots characterized by smaller magnitude. A higher ESL increases the impedance of the output capacitor branch, thus having an effect on the load transients roughly equivalent to a decrease of the capacitance. With the set-up (a) of Table 1, the total equivalent impedance seen by the LDO as output capacitor includes:

- a capacitance C_{16} = 10µF;
- an inductance L_2=100nH [**NOTE:** the resistor R_8 may have a parasitic inductance in the range from about 10nH to 50nH];
- an equivalent ESR composed of the ESR of the capacitor (from 5mΩ to 20mΩ), the 20mΩ resistance or the inductor L_2, the 100mΩ resistance R_8.

With the set-up (b) of Table 1, the total equivalent impedance seen by the LDO as output capacitor includes:

- a capacitance C_{17} = 47µF;
- an inductance L_1=1nH [**NOTE:** the resistor R_8 may have a parasitic inductance in the range from about 10nH to 50nH];
- an equivalent ESR composed of the ESR of the capacitor (from 5mΩ to 20mΩ), the 15mΩ resistance or the inductor L_1, the 1mΩ resistance R_7.

If the electronic load current slew-rate is low (below 0.01A/µs) the load transient response might be difficult to observe due to the wide bandwidth feedback loop gain. If the electronic load current slew-rate is high (above 10A/µs) the load transient response can be better observed. The output capacitor setup determines the magnituide and shape of the overshoot/undershoot output voltage transient, as shown in Figure 10 and 11. In real life applications, the R-L-C characteristics of the output impedance seen by the LDO regulators is influenced by the output capacitor, the impedance of the PCB layout traces and the impedance of the line connecting the regulator to the dynamic load. Any R-L-C element contributing to increase the output impedance causes an increase of the overshoot/undershoot surges magnitude.

In Test#2 we are interested in investigating the correlations among the load transient response of the TPS7A8300 LDO regulator, the characteristics of the equivalent output capacitor, and the load current slew-rate.

The different combinations of jumpers that can be selected for the equivalent output capacitor set-up may yield, sometimes, visible changes in the LDO regulator transient response, whereas in other conditions almost no changes are observed. As discussed above, the LDO regulator load transient response is determined by the load current slew-rate and by the influence of the R-L-C characteristics of the output capacitor on the LDO regulator voltage loop gain. When the load current-slew rate is low, the LDO regulator may have the time to compensate the current increase with a fast change of the pass device gate voltage, provided that the cross-over frequency of the voltage loop gain is high. A small C_{OUT} and a high ESR improve the bandwidth of the voltage loop gain. With high crossover and low current slew-rate, the load transient surges are very small. When the load current slew-rate is high, the LDO regulator may not be able to make a fast change of the pass device operating point and then the load transient response is determined by the characteristics of the equivalent output capacitor, as discussed above. Therefore, a small C_{OUT}, a high ESR, and a high ESL increase the magnitude of the output voltage load transient surges with high load current slew rate.

Experimental plots

The plots collected in these pages are samples of experimental measurements performed on the TPS7A8300 LDO regulator. They show the load transient response of the LDO regulator for different set-up of the output capacitor configuration (*see [3] for further details on the TPS7A8300 LDO regulator dynamic response*).

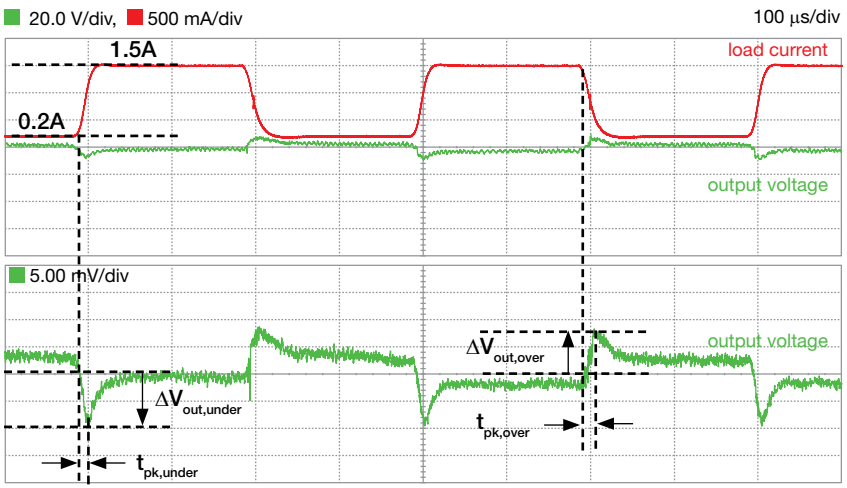


Figure 10. TPS7A8300 LDO regulator load transient response for: V_{in}= 1.8V, V_{out}=1.5V, I_{out}=0.2A↔1.5A, C_{out}=C_{16}=10µF, L_{out}=L_2=100nH, ESR_{out}=R_8=100mΩ

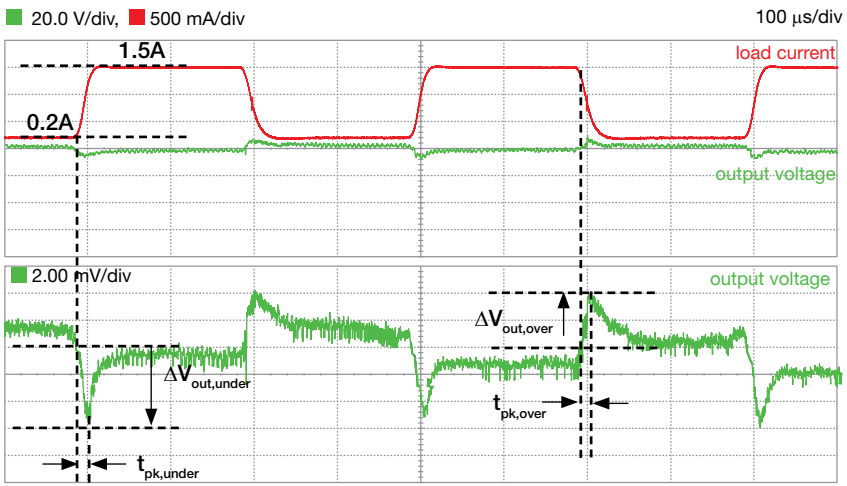


Figure 11. TPS7A8300 LDO regulator load transient response for: V_{in}= 1.8V, V_{out}=1.5V, I_{out}=0.2A↔1.5A, C_{out}=C_{17}=47µF, L_{out}=L_1=1nH, ESR_{out}=R_7=1mΩ

The plots of Figures 10 and 11 highlight the combined influence of the output capacitance, equivalent resistance and equivalent inductance on the load transient response of the TPS7A8300 LDO discussed in the previous section. The load current slew-rate in the above tests is about 0.35A/µs.

Experimental plots

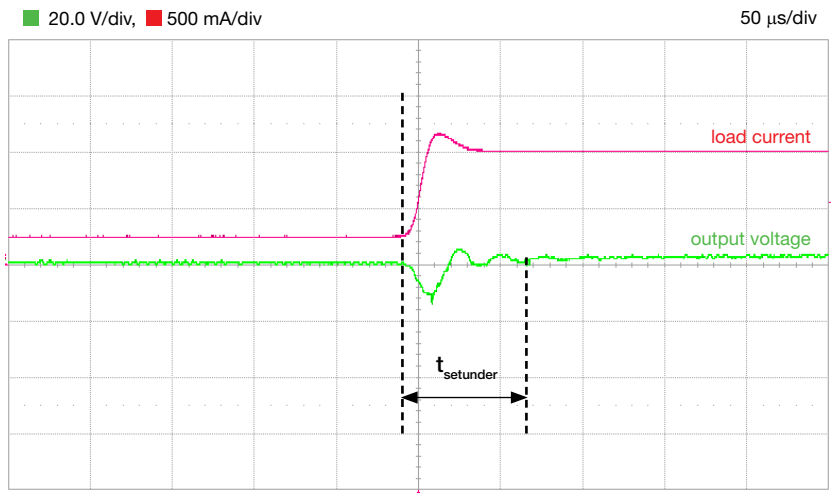


Figure 12. TPS7A8300 LDO regulator load transient response for: V_{in}= 2.5V, V_{out}=1.5V, I_{out}=0.25A→1.0A, C_{out}=C_{17}=47µF, L_{out}=L_1=1nH, ESR_{out}=R_7=1mΩ

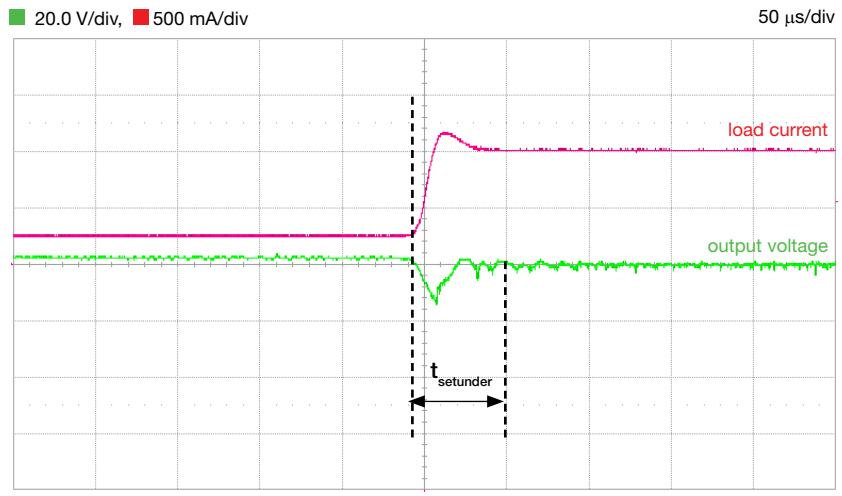


Figure 13. TPS7A8300 LDO regulator load transient response for: V_{in}= 1.8V, V_{out}=1.5V, I_{out}=0.2A→1.5A, C_{out}=C_{16}=10µF, L_{out}=L_1=1nH, ESR_{out}=R_8=100mΩ

The plots of Figures 12 and 13 highlight the combined influence of the output capacitance and equivalent resistance on the load transient response of the TPS7A8300 LDO discussed in the previous section. You can observe that the falling edge of the output voltage in Figure 13 looks almost linear and follows the load current rise. This is the effect of the higher ESR, which dominates the load transient shape during the fast load current swing, as highlighted in the *Theory Background* section. In Figure 12, instead, you can observe a different shape of the output voltage undershoot transient surge, which is dominated by the capacitance, due to the much smaller ESR and higher capacitance.

Appendix A

References

[1] Linear Regulators: Theory of Operation and Compensation, http://www.i.com/lit/an/snva020b/snva020b.pdf

[2] TPS7A4901 datasheet, http://www.ti.com/lit/ds/symlink/tps7a4901.pdf

[3] TPS7A8300 datasheet http://www.ti.com/lit/ds/symlink/tps7a8300.pdf

[4] LDO Regulator Stability Using Ceramic Output Capacitors, http://www.ti.com/lit/an/snva167a/snva167a.pdf

[5] LDO PSRR Measurement Simplified, http://www.ti.com/lit/an/slaa414/slaa414.pdf

[6] www.mathworks.com

[7] C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House

[8] www.omicron-lab.com

[9] Techniques for accurate PSRR measurements, http://www.ti.com/lit/an/slyt547/slyt547.pdf

[10] Simplifying Stability Checks, http://www, ti.com/lit/an/sbva026e/sbva026e.pdf

[11] A Topical Index of TI LDO Application Notes, http://www.ti.com/lit/an/sbva026e/sbva026e.pdf

[12] Technical Review of Low Dropout Voltage Regulator Operation and Performance, http://www.ti.com/lit/an/slva072/slva072.pdf

Appendix B

Manufacturers websites

ASJ,	*http://www.asj.com.sg/*
AVX,	*http://www.avx.com/*
Bourns,	*http://www.bourns.com*
Coilcraft,	*http://www.coilcraft.com/*
Diodes Incorporated,	*http://www.diodes.com/*
Kemet,	*http://www.kemet.com/*
Murata,	*http://www.murata.com/*
Nippon Chemi-Con,	*http://www.chemi-con.co.jp/*
ON Semiconductor,	*http://www.onsemi.com/*
Panasonic,	*http://industrial.panasonic.com/*
Philips Lumileds,	*http://www.philipslumileds.com/*
Rohm Semiconductor,	*http://www.rohm.com/*
Samsung,	*http://www.samsungsem.com/*
Samwha,	*http://www.samwha.com/*
Taiyo Yuden,	*http://www.t-yuden.com/*
TDK,	*http://product.tdk.com/*
TE Connectivity,	*http://www.te.com/*
Texas Instruments,	*http://www.ti.com/*
TT Electronics,	*http://www.ttelectronics.com*
Vishay,	*http://www.vishay.com/*
Yageo,	*http://www.yageo.com/*

TIuniversityprogram

Texas Instruments has been passionate about creating innovative technology solutions for more than 80 years. The TI University Program was established in 1982 and is a global program operating in 35 countries, multiple languages and impacting over hundreds of thousands of students every year. The TI University Program offers educators discounted tools, lab donations, and teaching materials so students can learn TI technology in the classroom and lab. From teaching materials to design projects, our advanced analog and embedded processing technologies fuel the passions of students and educators in university labs worldwide.

Coilcraft is your RF & Power Magnetic resource

Coilcraft understands that inductors can be difficult for students to understand, so we're committed to upporting you with the same tools and resources professional engineers rely on when designing power management and analog circuits.

Free product samples

Need some Coilcraft parts for your design project? We'll ship them today.

Industry's best design tools

Our powerful on-line tools will lead you to the perfect part quickly and easily.

Application notes

Our App Notes and Design Guides cover topics you might not learn about in class.

Free Power Management Lab Kit

This free parts tool kit helps instructors bring practical experience into the classroom.

Learn more @ Coilcraft.com/students

IMPORTANT NOTICE

TI Power Management Lab Kit ("TI-PMLK") – LDO Experiment Book is intended to introduce students to basic electronic theory and circuits through experiments outlined in this book. While Texas Instruments Incorporated and its subsidiaries (TI) update information periodically, it may not be current at the time you conduct experiments set forth in the book. You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in conducting experiments contemplated by this book. In addition to the terms below, your use of this book is subject to TI's Terms of Use located at http://www.ti.com/corp/docs/legal/termsofuse.shtml which are incorporated herein by this reference.

THE MATERIAL CONTAINED IN THIS BOOK (THE "CONTENT") IS PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THIS CONTENT, OR USE OF THIS CONTENT, WHETHER EXPRESS, IMPLIED, OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO THE CONTENT OR THE USE OF THE CONTENT. TI SHALL NOT BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF THE CONTENT OR USE OF THE CONTENT.

Certain books may contain experiments which contemplate the use of materials obtained from third parties and/or other materials that may be linked at www.ti.com. IN ALL SUCH INSTANCES, TI OFFERS NO WARRANTIES (EITHER EXPRESS OR IMPLIED), INDEMNIFICATION, OR SUPPORT OF ANY KIND WITH RESPECT TO THIRD PARTY MATERIALS AND, TO THE EXTENT PERMITTED BY LAW, ALL DISCLAIMERS OF WARRANTIES AND LIMITATIONS OF LIABILITY WITHIN THIS NOTICE WILL APPLY TO THE THIRD PARTY MATERIALS, AS WELL.

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.*
   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software
   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2. *Limited Warranty and Related Remedies/Disclaimers:*
   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.
   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3. *Regulatory Notices:*
   3.1 United States
      3.1.1 *Notice applicable to EVMs not FCC-Approved:*
      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *ncrease the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan. If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of

Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル

3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

4. *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 Safety-Related Warnings and Restrictions:

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*
   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*
   8.1 General Limitations. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.
   8.2 Specific Limitations. IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated

Texas Instruments

TI-PMLK

TI Power Management Lab Kit
LDO Experiment Book

The platform bar is a trademark of Texas Instruments. © 2016 Texas Instruments Incorporated.

SSQU006B
PMLK LDOEVM HWRev B

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated